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In re application of: **Burgener, et al.**

Serial No.: **10/658,154** Group Art Unit: **2816**

Filed: **September 8, 2003** Examiner: **Terry L. Englund**

For: **Low Noise Charge Pump Method and Apparatus**

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APPEAL BRIEF

Dear Sirs:

In accordance with the Notice of Appeal mailed May 12, 2008, the Appellants provide this Brief in support of the patentability of claims that remain rejected according to the Notice of Panel Decision from Pre-Appeal Brief Review issued June 26, 2008. An attached credit card authorization form provides the requisite fee for an attached petition for a 5-month extension of time to respond, and for the difference between the present fee under 37 CFR 41.20(b)(2) for filing a brief in support of the appeal, and that previously paid.

CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is PEREGRINE SEMICONDUCTOR CORPORATION, the assignee of record, a Delaware corporation based in San Diego, CA.

II. RELATED APPEALS AND INTERFERENCES

On information and belief, there are no related appeals or interferences. However, this is the third Appeal Brief submitted in respect of the ongoing appeal of this application. A first Appeal Brief was submitted May 15, 2006, but a paper deeming it noncompliant issued almost six months later, on November 2, 2006. An Amended Appeal Brief was accordingly submitted January 5, 2007. In order to revise some grounds of rejection, the Examiner reopened prosecution with a new Office Action issued on May 17, 2007; the Appellants responded with an amendment mailed on September 17, 2007. The application as then pending was finally rejected in an Office Action issued December 12, 2007, whereupon the Appellants submitted a Request for a Pre-Appeal Brief Review, together with a new Notice of Appeal, on May 12, 2008. A Notice of Panel Decision from Pre-Appeal Brief Review issued June 26, 2008 maintaining claim rejections, and the Appellants accordingly submit this new Appeal Brief.

III. STATUS OF CLAIMS

Claims 1-71 are pending. Claims 11, 21, 42 and 52 stand allowed, and Claims 26 and 62-65 stand allowable but objected to. Claims 1-10, 12-20, 22-25, 27-41, 43-51, 53-61 and 66-71 stand rejected.

Appeal is taken of rejections of Claims 1-10, 12-20, 22-25, 27-41, 43-51, 53-61 and 66-71.

IV. STATUS OF AMENDMENTS

No amendments are currently pending.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is an integrated circuit (IC) charge pump circuit, or a corresponding method, having a unique combination of features suitable to reduce excess electrical noise generated by conventional IC charge pump circuits. Subsection *V.A Problem Solved and Concept of the Claimed Subject Matter* sets forth essential context and an overview of the invention underlying the claimed subject matter, including remarks that are referenced in the Arguments subsection. Thereafter, the explicit elements of the independent claims are set forth in subsections *V.B.* to *V.H.*

V.A Problem Solved and Concept of the Claimed Subject Matter

Subsection *V.A.1* explains the noise problem that is addressed by the inventive subject matter. Subsection *V.A.2* describes a unifying inventive concept that underlies and leads to specific solutions for the problem, and further describes specific features that follow from the unifying inventive concept. The specific features serve to alleviate the noise problem when used as described in the specification, and distinguish embodiments of the invention from the prior art.

V.A.1 Well Known Noise Problem Has No Satisfactory Predictable Solution

Conventional IC charge pumps generate substantial electrical "noise." An integrated antenna switch developed by the Appellants needed an additional voltage to bias the active switch devices, but the noise generated by conventional IC charge pump designs caused the resulting switches to fail regulatory emissions requirements. Accordingly, it became imperative for the Appellants to develop a charge pump that produced far less electrical noise than prior art charge pump designs. Unfortunately, because noise is an unintentional result of circuit operation, there is no predictable, analytic procedure to determine, and then avoid, the cause of the noise.

A number of prior art references address the problems of noise generated by charge pumps. Of the eighty-two references of record that include an integrated circuit charge pump (of ninety-four total references of record), at least nine address noise issues; seven of those propose useful, identifiable solutions. The solutions proposed include balancing opposing current sources and reducing operational duty cycle (D1); regulating input current on both phases of the clock (D2, D6);

using constant frequency operation (also D2, D6); turning transistors on more slowly than turning them off (D3), separating switching circuitry from input and output during certain switching events (also D3); disabling "boosting" circuitry during normal operation (D27, D29); coupling the switching circuitry to ground only through a current limiting circuit (D50); and using a current mirror to increase output capacitance (D80).

References D1, D2, D3, D6, D27, D29, D50 and D80 demonstrate several important points. First, they show that noise problems are longstanding problems in the art. Second, their approaches are not, in general, analytical, supporting a conclusion that noise problems cannot be readily addressed by predictable, analytic techniques. Indeed, only one solution, increasing the output capacitance, is developed analytically. Increasing the output capacitance is uninteresting because it is very well known for reducing noise on the charge pump output, yet it fails to control the noise that threatens to cause the Appellants' devices to fail to meet emission levels mandated by regulation. It is inadequate for the Appellants' purposes, because although it reduces output ripple voltage, it permits or even encourages other, less measurable sources of noise generation and propagation. For example, the low output impedance produced by a large output capacitance is likely to cause switching current spikes to circulate through the components of the charge pump, which apparently causes noise to be propagated to devices that effect emissions. Because the mechanisms of noise generation and propagation in integrated circuits are not well understood, the explanation provided is necessarily somewhat conjectural. Taken together, these references demonstrate that the problem of noise is well known but not well understood or easily prevented.

V.A.2 Inventive Concept Differs Radically from Prior Art Teaching

The most important fact about all of the prior art references identified above that address the problem of noise generated by a charge pump is that each and every clock waveform they describe using for the charge pump is square (or, equivalently, rectangular or pulse). As such, in all of the known prior art that addresses the problem of noise, there is not the least hint of a solution comprising the unifying concept that leads to the Appellants' claimed subject matter: significantly slowing the charge pump clock waveform compared to all previous practice, *i.e.*, compared to all known integrated circuit charge pump prior art. The Appellants teach that **making the charge**

pump clock waveform less square and more rounded, sometimes to the point of **being substantially sine-like**, can dramatically reduce the electrical noise emissions caused by a charge pump.

Every prior art solution that addresses the problem proposes that a square clock waveform be used that is the diametric opposite of the Appellants' inventive concept of using a drastically slowed charge pump clock, and none of the very extensive charge pump prior art demonstrates the Applicants' inventive solution, even by accident. As such, the Appellants' inventive solution to the problem caused by noise is not only unpredictable, but it is a radical departure from the teaching and practice of the prior art. The most skilled people in the art have all failed to teach or suggest the unifying inventive concept of slowing the charge pump clock that underlies the Appellants' claims. They have not suggested the concept for any purpose, let alone for the purpose of solving the noise problem.

Although a square charge pump clock waveform is by far the most common, it is true that not all of the vast number of prior art charge pumps clocks require a square output waveform. No "square wave" is ever perfectly square; and some clock generation circuits that are easy to fabricate tend to create an output that is less than perfectly square. Some prior art designs tolerate a clock waveform that is less than perfectly square; for example, several references describe clock waveforms that are trapezoidal in nature. Current starved ring oscillators, in particular, tend to generate trapezoidal waveforms, and their outputs tend to become less square and more trapezoidal as the number of inverter stages is reduced. One odd design even illustrates use of a sawtooth waveform.

However, there is no evidence whatsoever that use of slow, well rounded clock waveforms are considered desirable in the prior art. In contrast, the few examples of waveforms that are somewhat less than square appear to be merely tolerated, not desired. No suggestion is seen anywhere in the prior art of record to suggest that slowing the charge pump clock is desirable for any reason, let alone for suppressing noise.

Given the extensive and crowded nature of charge pump prior art, the overwhelmingly predominant use of square clock waveforms, in combination with a complete absence of any

suggestion that a slow clock waveform is desirable, is compelling evidence that fast (sharp-edged) clock waveforms are strongly preferred, and that inventors of the prior art actively avoided permitting the clock waveform to be too slow and rounded. That is believed to be the reason that no prior art of record suggests creating a clock using a current starved ring oscillator having less than five stages, and why the Hara reference, the only prior art known to address the desirable range of the number of stages of a ring oscillator for a charge pump, expressly suggests that a current starved ring oscillator for a charge pump clock should have at least five stages.

The Appellants teach slowing down a charge pump clock to such a degree that their preferred clock generator, a current starved ring oscillator having only three stages, falls outside the bounds of any example in the crowded field, and even outside the bounds of the express teaching of an appropriate range for a given number of stages. The Appellants were not simply avoiding the prior art in their design; indeed, they were completely unaware of the Hara reference teaching that at least five stages should be used in a ring oscillator for use in a charge pump. Thus, Hara provides independent evidence that Appellants have designed and innovated away from the teaching of the prior art in respect to the charge pump clock and waveform.

V.A.3 Claimed Features Are Undesirable EXCEPT to Implement the Invention

The inventive concept underlying the Appellants' invention is slowing down the charge pump clock far more than has been tolerated in prior art IC charge pumps. As noted above, this unpredictable solution is radically different from any teaching in the prior art. However, "slower" and "rounded" are relative terms which are difficult to define in a claim. The Appellants have defined one set of waveforms that satisfy this requirement, and these are well distinguished over the prior art. Namely, in some embodiments of an IC charge pump clock, the Appellants require having a "substantially sine-like" output waveform. However, quite aside from the Examiner's objections to these claims, they do not adequately protect the Appellants' invention. Many embodiments have suitably "slow" clock waveforms that may not, however, be "substantially sine-like." As such, the Appellants wish to define the scope of the invention in terms of specific features that had not been and would not have been employed in the prior art except in accordance with the teaching of the Appellants for the purpose of reducing noise.

IC charge pumps having the claimed distinguishing features are not found in the prior art, as demonstrated by the Examiner's inability to identify any prior art that anticipates any claim. Moreover, IC charge pumps would not have been modified to employ the claimed features, because the prior art teaches widely practiced alternatives that are more flexible and less expensive to implement, especially for CMOS integrated circuits, than are the solutions taught and claimed by the Appellants.

At the time of the invention, the features taught and claimed by Appellants were demonstrably undesirable from the perspective of a person of ordinary skill in the art who had no knowledge of Appellants' disclosed solution to the problem created by excess noise.

Current starved ring oscillators having no more than three stages were undesirable because they produce a clock that is too slow for prior art design goals. Capacitive coupling of clock signals to switches that they control was undesirable due to the large IC area required to implement capacitive coupling and associated biasing impedances. This is particularly true in CMOS ICs that have tremendous flexibility for coupling clock signals in any phase and to any part of the circuit using extremely small active devices. Passive coupling, such as used by a simple connection, makes logical sense if it can be made to work. However, no passive coupling method (other than the expensive capacitive coupling taught by the Appellants) is seen in the prior art that does not cause undesirable simultaneous conduction in the charge transfer switches, when all of the switches (TCCSs) are actively controlled.

So far as can be ascertained by the extensive prior art of record, the constraints and capabilities of CMOS IC fabrication render certain design features so desirable that they have been employed in every single CMOS IC charge pump ever fabricated. The extensive evidence of record supports a conclusion that no CMOS IC designs have ever employed capacitive coupling between a charge pump clock circuit and the transfer switches that is controlled thereby.

To be sure, capacitive coupling would make sense if, like the Appellants, a designer desired to replicate a slow analog waveform at switch control nodes without constantly regenerating the waveform, because CMOS IC devices are less adept at coupling such slow analog waveforms. But that circumstance would only arise if a designer first had the motivation to use a slow analog clock

waveform, rather than a conventional digital waveform, in a charge pump clock. This underlying inventive concept, however, was known only to the Appellants until they disclosed it in the subject patent application.

At the time of the invention, Appellants claimed distinguishing features were unused and unwanted. Only in view of Appellants' inventive solution to the problem of excessive charge pump noise were any of the claimed features desirable at the time of the invention. Of course the claimed features are possible to implement. The Appellants could not have claimed them if they were impossible to implement. There are only a few basic elements in electronics, so if the Examiner is free to pick and choose from any element described in the prior art of electronics, he will have no trouble substituting a component from an unrelated circuit into a prior art charge pump in accordance with the road map set forth in the Appellants' claims. However, those features were not implemented, and would not have been implemented as claimed in the relevant art of IC charge pumps, and especially in CMOS IC charge pumps. As such, the Appellants are properly entitled to patent protection for the claimed combinations.

V.A.4 Benefit of the Claimed Features Is Entirely Unexpected

As noted above, the claimed features are not found in the extensive prior art of charge pumps, leading to the reasonable conclusion that the claimed features were considered unsuitable for charge pumps. As also acknowledged, the claimed features were at no time beyond the technical capacity of skilled persons. They were not done, however, because of perceived undesirable aspects, in combination with an utter lack of positive reason to employ the claimed feature combinations.

Of course, the Appellants did not decide to design a charge pump using capacitors to couple the charge pump clock to the TCCSs, and then discover that such a design reduces noise and is therefore desirable. Even the Appellants could not have predicted that most of the significant distinguishing claimed features would assist in reducing noise generation.

Even after the fact it is difficult to see how using a three stage current starved ring oscillator to generate the charge pump clock, or coupling a single-phase clock output to TCCSs passively, or without increasing its voltage rate of change, or capacitively coupling the clock output to the TCCSs

without increasing its rate of voltage change, such as by capacitive coupling, help solve the longstanding problem of excess electrical noise generation by charge pumps.

Nobody could have expected such effects, because the benefits follows from a further feature that is itself not reasonably predictable, and certainly was not previously taught: namely, that the charge pump clock should be slowed down compared to all conventional charge pump clocks. Once it is realized that a fast clock signal is a cause of noise, the contribution of the other features becomes easier to understand by considering how each facilitates the use of a slow clock signal throughout the charge pump. Without the entirely new inventive concept introduced by the Appellants in their application for patent, the noise reducing effects of the claimed feature combinations are startlingly unexpected. Even in view of the inventive concept, which was not available to skilled persons at the time of the invention, the results are unexpected, though at least easier to understand.

The salutary effects achievable through the claimed feature combinations are startlingly unexpected. This fact strongly supports a conclusion that such feature combinations are nonobvious. The unexpectedness of the advantages also explains why the feature combinations were avoided for decades of IC charge pump development, even though they are not for the most part technically difficult to do.

The pending independent claims, each of which include at least one of such distinguishing features, are described below, grouped according to an important distinguishing feature.

V.B Charge Pump Driven by a Three stage Current Starved Ring Oscillator

Apparatus Claim 1 and method Claim 43 each define a charge pump driven by a current starved ring oscillator clock that has fewer inverter stages than has previously been thought suitable.

V.B.1 Claim 1

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 3-12, and examples: +/- outputs in Fig. 2 at 216/218 and/or 224/226, Fig. 3 at 316/318, Fig. 4 at 404/634, and Fig. 7 at 404/710; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9

as described from page 16 line 27 to page 18 line 3; and 1014/1016 in Fig. 10) **within a circuit, comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12 and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 702 in Fig. 7, 902 and 912 in Fig. 9, and 1012 in Fig. 10);

b) **a plurality of transfer capacitor coupling switches** ("TCCSs," see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, page 15 lines 17-27, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, diode-connected FETs 704 and 706 in Fig. 7, switches 800 and 830 in Figs. 9 and 10), **each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output** (see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - outputs 354, 356, 362 and/or 364 in Fig. 3, output 524 in Figs. 6 and 7, and clock 802 in switch modules 800 and 830 of Fig. 8, as used in Figs. 9 and 10); **and**

c) **a charge pump clock generating circuit** (see, *e.g.*, page 8 line 29-page 9 line 2, page 12 lines 4-26, and examples - 350 in Fig. 3, 500 in Fig. 5) **including a ring oscillator** (*e.g.*, page 12 lines 4-26, ref. 500) **comprising an odd number of not more than three inverting driver sections** (see, *e.g.*, page 12 lines 5-10 and examples - 508/502/514, 510/504516, 512/506/518 of Fig. 5) **cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section** (*e.g.*, 508/502/514) **is next after a last driver section** (*e.g.*, 512/506/518) **and one of the driver section outputs** (*e.g.*, 512/506/518 in Fig. 5) **constitutes a particular charge pump clock output** (see, *e.g.*, page 9 lines 26-29, page 10 lines 14-17, page 12 lines 23-25, and examples - 354, 356, 362 or 364, and 524) **controlling at least one of the transfer capacitor coupling switches** (see, *e.g.*, page 9 lines 26-29, page 12 lines 4-15, page 13 line 30-page 14 line 2, and examples - Fig. 5, paragraph 49; 602, 604, 608, or 610 of Fig. 6; 704 or 706 of Fig. 7; generally, switch circuits 800, 830 of Fig. 8 as used in Fig. 9 or Fig. 10), **and wherein each driver section includes**

i) **circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output** (see, *e.g.*, page 12 lines 5-15, and examples - 508, 510 and 512 of Fig. 5; exemplary details 426 of Fig.4), **and ii) circuitry configured as an active current limit**

to limit a rate of fall of voltage at the driver section output (see, *e.g.*, page 12 lines 5-15, and examples - 514, 516, 518 of Fig. 5, exemplary details 430 of Fig. 4);

d) **wherein the plurality of transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source** (see, *e.g.*, page 7 lines 3-21, page 13 line 30-page 14 line 16, page 16 line 27-page 18 line 3, and examples - +/- source connections 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times** (see, *e.g.*, page 12 line 27-page 13 line 2, and page 14 lines 17-28, paragraphs 51, 57).

V.B.2 Claim 43

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **by alternately transferring charge from a source voltage** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 702 in Fig. 7, 902 and 912 in Fig. 9, and 1012 in Fig. 10)**, and from the TC to the output supply, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a discharging switch circuit** (see, *e.g.*, page 12 line 31-page 13 line 2, page 16 line 27-page 18 line 3, and examples - 608 or 610 of Fig. 6; 706 of Fig. 7; various in Fig. 9; 800 in Fig. 10) **under control of a first charge pump clock output** (see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - 354, 356, 362 or 364 of Fig. 3, 524 of Fig. 5);

b) **limiting source current provided to each inverting driver** (see, *e.g.*, page 12 lines 5-8, and examples - 502, 504, 506 of Fig. 5) **output node of a current starved ring oscillator** (*e.g.*, 500 of Fig. 5) **having not more than three inverting driver stages within a first charge pump clock generator circuit** (see, *e.g.*, page 12 lines 20-21, and examples - 350 of Fig. 3, 500 of Fig. 5) **by means of a corresponding source current-limiting circuit** (see, *e.g.*, page 12 lines 6-8 and examples - 508, 510, 512 of Fig. 5); **and**

c) **limiting sink current drawn from each of the inverting driver output nodes by by means of a corresponding sink current-limiting circuit** (see, *e.g.*, page 12 lines 8-10, and examples - 514, 516, and 518 of Fig. 5);

wherein the inverting driver output node (*e.g.*, 524 of Fig. 5) **of one** (506 of Fig. 5) **of the not more than three inverting driver stages of the first charge pump clock generator circuit is the first charge pump clock output**.

V.C Charge Pump Driven by a Substantially Sine-Like Generated Clock Output

Claim 12 (apparatus) and Claim 28 (method) are distinguished from the prior art in part by an output waveform that differs significantly from waveforms of all previous integrated charge pump clock outputs, and which is contrary to the goals and practices of prior art charge pump design.

V.C.1 Claim 12

Charge pump apparatus within a monolithic integrated circuit for generating an output voltage supply (see, *e.g.*, page 7 lines 3-12, and examples: +/- outputs in Fig. 2 at 216/218 and/or 224/226, Fig. 3 at 316/318, Fig. 4 at 404/634, and Fig. 7 at 404/710; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9 as described from page 16 line 27 to page 18 line 3; and 1014/1016 in Fig. 10), **comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 702 in Fig. 7, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **coupled alternately between source connections** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection examples - 208/210 of Figs. 2 and 3; 402/404

in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **and output connections** (*e.g.*, references as previously noted for output voltage supply);

b) **a plurality of active switches** (see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, switches 800 and 830 in Figs. 9 and 10), **each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output** (not shown in Fig. 2; see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - outputs 354, 356, 362 and/or 364 in Fig. 3, output 524 in Fig. 6, and clock 802 in switch modules 800 and 830 of Fig. 8, as used in Figs. 9 and 10) **to couple charge, which is not substantially conducted by the charge pump clock output, from the source connections to the output connections;**

c) **a charge pump clock generating circuit** (see, *e.g.*, page 8 line 29-page 9 line 2, page 12 lines 4-26, and examples - 350 in Fig. 3, 500 in Fig. 5) **including an active driver circuit** (*e.g.*, 512/506/518 of Fig. 5) **configured to both source current to and sink current from the charge pump clock output** (524) **to cause a voltage waveform of the charge pump clock output to be substantially sine-like** (paragraph 50 at page 12, lines 16-26) **due to**

i) **circuitry** (see, *e.g.*, page 11 lines 22-25, page 12 lines 6-18, and examples - 512 in Fig. 5, exemplary details 426 in Fig. 4) **configured to limit source current provided by the active driver circuit to the charge pump clock output, and**

ii) **circuitry** (see, *e.g.*, page 11 lines 22-29, page 12 lines 8-18, and examples - 518 in Fig. 5, exemplary details 430 in Fig. 4) **configured to limit current sunk from the charge pump clock output by the active driver circuit.**

V.C.2 Claim 28

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in

Fig. 9; 1014/1016 in Fig. 10) **from a charge pump incorporated within a monolithic integrated circuit by transferring charge from a source voltage** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS")** (see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, switches 800 and 830 in Figs. 9 and 10) **circuit is a switching circuit of the charge pump configured to couple the TC to a supply** (*e.g.*, source, output or intermediate; a supply has two terminals) **under control of a charge pump clock** (not shown in Fig. 2; see, *e.g.*, page 12 line 29-page 13 line 2, page 13 line 30-page 14 line 4, and examples - outputs 354, 356, 362 and/or 364 in Fig. 3, output 524 in Fig. 6, and clock 802 in switch modules 800 and 830 of Fig. 8, as used in Figs. 9 and 10) **, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a discharging TCCS circuit** (see, *e.g.*, page 12 line 31-page 13 line 2, page 16 line 27-page 18 line 3, and examples - [220 and 222] and/or [212 and 214] in Fig. 2; [312 and 314] in Fig. 3; [608, 610 and 616] in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of a first charge pump clock output** (not shown Fig. 2; *e.g.*, 362 or 364 Fig. 3; 524 Figs. 6 and 7; 802 of Fig. 8 in Figs. 9 and 10)**; and**

b) **actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions** (see, *e.g.*, page 12 lines 23-26, and examples - 512, 518 and 524 in Fig. 5) **such that a voltage of the first charge pump clock output is substantially sine-like** (paragraph 50, page 12 lines 16-26).

V.D Single-Phase Clock Coupled Passively without Transfer Current to TCCSs

It will be useful, first, to describe a distinction between two families of charge pumps, which reflects important differences in the function of the circuit identified as the "clock." The claims in this subsection cover only "control only" charge pumps, and do not cover "direct TC drive" charge

pumps. Distinctions between these families, together with claim language establishing such distinction, are described in the following remarks.

V.D.1 Two Types of Charge Pumps

The essence of a charge pump method is first "pumping charge" into a "transfer capacitor" ("TC") by connecting it to a source supply, then disconnecting the TC from the input supply and connecting it instead to an output supply, into which the TC will then "pump" its charge. Because the TC is alternately connected to different supplies, it is often said to "fly" between them, and TCs are sometimes referred to as "fly capacitors" in the literature. Only charge pumps fabricated entirely on an integrated circuit (IC charge pumps), and only those that are controlled by a charge pump clock, are described and claimed in pending claims of the subject application.

Because slowing and changing the shape of the charge pump clock is central to the Appellants' solution for reducing the noise unintentionally produced by charge pump operation, the charge pump clock is a focus of many claims. The charge pump clock controls TC charging switches ("TCCSs"), and the nature of the clock output waveform significantly affects practical implementations of coupling between the charge pump clock and the TCCSs it controls. Therefore, aspects of such coupling characterize many claims as well.

When considering such important distinguishing features of the pending claims, confusion will be reduced if two types or classes of charge pumps are clearly recognized. Each claim encompasses either one or both classes of charge pumps, as may be seen by language specifying or excluding one class or the other, or by the absence of such language, in which case both classes are encompassed.

The two types or classes of charge pumps are distinguished by the relationship between the charge pump clock output and a transfer capacitor (TC).

In a first type, charge into and out of a TC is directly driven by a charge pump clock output. In a second type, by contrast, the charge pump clock does not directly drive current into or out of a TC. Instead, the current into and out of a TC is driven by TC charging switches (TCCSs), and the charge pump clock output is exclusively a control signal, which is applied to one or more TCCSs.

Any current into a TC from a charge pump clock of the second type is incidental, *de minimus* and/or parasitic. Substantially all of the TC charge and discharge current is provided by one or more TCCSs controlled by a charge pump clock that does not provide significant charge to the TC. The first type of charge pump may be referred to as having a "direct TC drive" charge pump clock, or simply as being a "direct TC drive" charge pump. The second type may be referred to as having a "control only" charge pump clock, or as being a "control only" charge pump. Most charge pumps use only one or the other of these two classes of clocks, because the architecture and operation of the two types of circuit is different and not readily mixed.

The application as filed provides distinctions between the two different types of charge pumps implicitly, and by means of distinguishing language in the claims. Express designation of these two types of charge pumps has been set forth subsequently in order to provide a conceptual framework to understand elements in claims that limit the type of charge pump to which the claim applies. For example, because a preferred embodiment of the invention was a "control only" charge pump, many claims include language that effectively excludes "direct TC drive" charge pumps. Many other claims cover both types of charge pumps. As such, though an effort is made in this Brief to refer consistently to "direct TC drive" and "control only" charge pumps, other designations may have been used inadvertently; and certainly some different designations have been used in earlier efforts to clarify the conceptual and practical distinctions between these two classes of charge pumps.

As noted, "control only" charge pump clock(s) provide only control signals to transfer capacitor coupling switches ("TCCSs"), which in turn convey the current to the transfer capacitor ("TC"), and do not provide significant current to the TC or the output. Examples of "control only" charge pumps include the Appellants' Figs. 2, 3, 6, 8 and 9, as well as Imamiya (Fig. 10), Tasdighi (Figs. 2, 4, 7-9), Nork (Figs. 2A-9A), Bingham '774 (Figs. 1A, 1B and 3), Butler (Figs. 1-3) and Yokomizo (Figs. 1-5). At least one of each of the charge and discharge TCCSs is generally actively controlled by a clock output in a "control only" charge pump, and often four TCCSs in a bridge are all actively controlled via their respective control nodes. Because the TCCSs in a "control only" charge pump are often arranged in a bridge around the TC, the term "bridge-type" is sometimes used to describe charge pumps of that topology.

"Direct TC drive" charge pump clocks conduct charge directly in order to generate the output supply. In fact, the capacitor coupled directly to such "clock" typically is the transfer capacitor. No TCCSs need appear to be "actively controlled" by a "direct TC drive" clock. Rather, the TCCSs are commonly passive devices, such as diodes or diode-connected FETs, reacting only to applied voltages to switch on (forward biased) or switch off (reverse biased). Examples of this family of charge pumps include Imamiya (Fig. 5, each C is a TC); Vaughn (Fig. 1; TCs 28, 40, 49, 53), Backes (Figs. 2-3, TCs C2, C3), Arakawa (Fig. 3, Co is TC) and Doluca (Fig. 3, TCs C1, C2), among others.

In a "direct TC drive" charge pump, TCCSs may appear to be passively, and indeed capacitively, coupled to the clock output. That is because the clock of such a charge pump performs the completely different function of providing current to the TC, rather than merely providing control signals to the TC. The TC performs a dual function as TC and coupling device. Due to this functional difference between the two families of charge pumps, comparison of "apples to apples" in charge pumps often requires recognition of the distinction between these families. To avoid confusion, therefore, Claims 18 and 49 are limited to "control only" charge pumps. More explicitly, they are restricted to having clocks whose outputs do not directly provide significant current to the TC or to the output.

V.D.2 Claim 18

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit, comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10);

b) **one or more source switching devices** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10) **disposed in series between the transfer capacitor and a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection

examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to convey transfer current to the transfer capacitor from the voltage source when conducting;**

c) **one or more output switching devices** (see, *e.g.*, page 7 lines 7-10, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - [220 and/or 222] and/or [212 and/or 214] in Fig. 2; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **disposed in series between the transfer capacitor and the output voltage supply to convey transfer current from the transfer capacitor to the output voltage supply when conducting; and**

d) **a charge pump clock generating circuit** (*e.g.*, 500 in Fig. 5) **configured to provide a single-phase charge pump clock output** (see, *e.g.*, page 12 lines 27-28, page 14 lines 26-28, and examples - 524 from Fig. 5 for Fig. 6, 802 in Fig. 8 for Figs. 9-10) **coupled passively** (exclusively via passive devices, see, *e.g.*, page 13 line 30-page 14 line 12, page 16 lines 12-13, and examples - 618 and 620 in Fig. 6, 812 for switches 800 in Figs. 9-10) **without conveying substantial transfer current** (*i.e.*, not a direct-drive clock), **to control nodes** (*e.g.*, FET gates, isolated from TCs) **of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively** (*e.g.*, via 622 and 624 of Fig. 6, or 822 of switches 830 in Figs. 9-10), **without conveying substantial transfer current, to control nodes** (FET gates, isolated from TCs) **of each of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices, wherein the charge periods alternate with, and do not overlap, the discharge periods.**

V.D.3 Claim 49

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit by alternately transferring charge from a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source

connection examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10), **and from the TC to the output supply, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a TC discharging switch** (see, *e.g.*, page 7 lines 7-10, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - [220 and/or 222] and/or [212 and/or 214] in Fig. 2; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of a single phase charge pump clock output** (see, *e.g.*, page 12 lines 27-28, page 14 lines 26-28, and examples - 524 from Fig. 5 for Fig. 6, 802 in Fig. 8 for Figs. 9-10) **that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC** (not shown Fig. 2; see, *e.g.*, page 13 lines 24-29, and examples - capacitors 622 and 624 to gates of FETs 608 and 610, respectively, in Fig. 6; capacitors 812 to gates of FETs 808, or capacitors 822 to gates of FETs 818 of Fig. 8 for Figs. 9-10); **and**

b) **coupling the TC to the voltage source via a TC charging switch** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10), **during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch** (not shown Fig. 2; coupled exclusively via passive devices, see, *e.g.*, page 13 line 30-page 14 line 12, page 16 lines 12-13, and examples - 618 and 620 in Fig. 6, 812 for switches 800 in Figs. 9-10, to control nodes such as a gate of FET 602 or FET 604 in Fig. 6, and a gate of a FET 818 or a gate of a FET 808 of Fig. 8 for Figs. 9-10).

V.E Claim 21: Discharging Switch Device Area Disparity

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a circuit, comprising:**

a) a transfer capacitor ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10);

b) one or more source switching devices (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10) **disposed in series between the transfer capacitor and a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via 524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10);

c) a first output switching device (see, *e.g.*, page 13 lines 3-16, and examples - FET 314 of Fig. 3, FET 610 of Fig. 6) **having a first device area disposed between a first terminal** (*e.g.*, right side of 202 in Fig. 3, right side of 606 in Fig. 6) **of the transfer capacitor and the output voltage supply** (*e.g.*, Vo- 318 of Fig. 3, Vo- 634 of Fig. 6), **and a second output switching device** (see, *e.g.*, page 13 lines 3-16, and examples - FET 312 of Fig. 3, FET 608 of Fig. 6) **disposed between a common reference connection** (*e.g.*, Vo+ 316 of Fig. 3, common 404 of Fig. 6) **of the output voltage supply and a second terminal** (*e.g.*, left side of 202 in Fig. 3, left side of 606 in Fig. 6) **of the transfer capacitor opposite the first terminal of the transfer capacitor, having a second device area that is greater than double the first device area; and**

d) a charge pump clock generating circuit (see, *e.g.*, page 12 lines 27-28 *et seq.*, and example 500 of Fig. 5 for 524 of Fig. 6, or for 802 of Figs 7 and 8 as used in Figs. 9 or 10) **configured to provide a single-phase charge pump clock output coupled to all of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled to all of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices.**

V.F Clock Coupled Capacitively to an Isolated Control Node of a TCCS

This preferred coupling technique solves several problems of implementation, and would not be used for IC charge pumps except as taught by the Appellants. The highly capable but tiny CMOS switches available on ICs renders bulky solutions like capacitors highly undesirable for coupling the clock to the switches, so capacitors would not be used, except as necessary. They are necessary for storing and transferring charge, but that reason exists only for transfer capacitors. No reason to couple the clock to switches via a capacitor that is not a transfer capacitor existed at the time of the invention, aside from the need to convey a slow, analog clock signal that itself was anathema to IC charge pump designers prior to the Appellants' invention.

V.F.1 Claim 24

Charge pump apparatus for generating an output voltage supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit, comprising:**

a) **a transfer capacitor** ("TC," also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **for conveying charge from a voltage source** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source connection examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to the output voltage supply;**

b) **one or more source switching devices** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10) **disposed in series between the transfer capacitor and the voltage source, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source;**

c) **one or more output switching devices** (see, *e.g.*, page 7 lines 7-10, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - [220 and/or 222] and/or [212 and/or 214] in Fig. 2; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **disposed in series between the transfer capacitor and the output voltage supply, each having a corresponding control node** (not shown Fig. 2; see, *e.g.*, page 13 lines 24-29, and examples - gates of FETs 608 and 610 in Fig. 6; gates of FETs 808 or FETs 818 of Fig. 8 for Figs. 9-10) **that is substantially isolated from both the transfer capacitor and the voltage source** (unlike, *e.g.*, gates of 704 and 706 in Fig. 7)**; and**

d) **a capacitive coupling circuit** (see, *e.g.*, page 13 line 30-page 14 line 1, and examples - 618/626, 620/628, 622/630 and/or 624/632 in Fig. 6; 812/810 and/or 822/820 in Fig. 8 for Figs. 9-10) **coupling a charge pump clock output** (*e.g.*, 524 in Fig. 6, 802 in Fig. 8 for Figs. 9-10) **to one of the control nodes corresponding to a source switching device** (whether or not referred to in (b)) **or to an output switching device** (whether or not referred to in (c))**.**

V.F.2 Claim 60

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **within a monolithic integrated circuit by alternately transferring charge for the output supply from a source voltage** (see, *e.g.*, page 7 lines 3-21, page 12 lines 27-31, page 16 line 27-page 18 line 3, and examples - +/- source connections 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10)**, and from the TC to the output supply, the method comprising:**

a) **coupling a first charge pump clock output** (*e.g.*, 524 in Fig. 6, 802 in Fig. 8 for Figs. 9-10) **to a control node** (see, *e.g.*, page 13 lines 24-29, and examples - gates of switching FETs) **of a TC charging switch** (see, *e.g.*, page 7 lines 5-7, page 12 lines 29-31, and examples - 204 and/or 206 in Fig. 2; 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig.

10) **via a first capacitive coupling network that does not conduct a significant portion of the charge for the output** (see, *e.g.*, page 13 line 30-page 14 line 12, page 14 lines 29-31, R*C product preferably about 10*period of clock, hence insignificant current, and gates are isolated from TC and supply; and examples - 618/626, 620/628, 622/630 and/or 624/632 in Fig. 6; 812/810 and/or 822/820 in Fig. 8 for Figs. 9-10);

b) **coupling the TC to the source voltage during charge periods via the TC charging switch under control of the first charge pump clock output** (see, *e.g.*, page 7 lines 3-21 and page 12 lines 27-31;

c) **coupling a second charge pump clock output** (may be like 350 of Fig. 3 in having plural outputs or phases, so may be another or the same of, *e.g.*, 524 in Fig. 6, 802 in Fig. 8 for Figs. 9-10,) **to a control node** (*e.g.*, gate of switching FET) **of a TC discharging switch** (see, *e.g.*, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - 312 and/or 314 in Fig. 3; 608 and/or 610 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 800 in Fig. 10) **via a second capacitive coupling network** (see, *e.g.*, page 13 line 30-page 14 line 12, and examples - 622/630 and/or 636/638/624/632 in Fig. 6; 822/820 or 812/810 in Fig. 8 for Figs. 9-10) **that does not conduct a significant portion of the charge for the output** (see, *e.g.*, page 14 lines 29-31, R*C product preferably about 10*period of clock, hence insignificant current, and gates are isolated from TC and supply, hence insignificant current); **and**

d) **coupling the TC to the output supply via the TC discharging switch during discharge periods nonconcurrently alternating with the charge periods under control of the second charge pump clock output** (see, *e.g.*, page 7 lines 3-21, page 12 line 31-page 13 line 2, page 16 lines 16-29-page 17 lines 17-19).

V.G Claim 42: Switch AC Impedance Disparity with Clock dV/dt Limit

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **from a charge pump by transferring charge from a source voltage** (see, *e.g.*, page 7 lines 3-12, page 16 line 27-page 18 line 3, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6, and Fig. 7 via

524/506/512 of Fig. 5; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10) **alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS") circuit** (see, *e.g.*, page 7 lines 5-10, page 8 lines 1-14, page 12 line 29-page13 line 7, page 13 lines 24-28, page 15 lines 17-27, and examples - S1-S6 in Fig. 2, FETs 304, 306, 312 and 314 in Fig. 3, FETs 602, 604, 608 and 610 in Fig. 6, switches 800 and 830 in Figs. 9 and 10) **is a switching circuit of the charge pump configured to couple the TC to a supply** (any of the supplies noted above, or a further one such as represented in Fig. 9) **under control of a charge pump clock** (*e.g.*, 354, 356, 362 and/or 364 of Fig. 3; 524 of Fig. 6) **, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a discharging TCCS circuit** (see, *e.g.*, page 10 lines 1-9, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - FETs 312 and/or 314 of Fig. 3; 608 and/or 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of a first charge pump clock output** (*e.g.*, 364 or 362 of Fig. 3, or 524 of Fig. 6);

b) **actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions** (see, *e.g.*, page 12 lines 4-26, and examples - current sources 512 and 518 of Fig. 5);

c) **coupling a first terminal** (*e.g.*, left side of 202 of Fig. 3 or 606 of Fig. 6) **of the TC to a common reference connection of the output supply** (*e.g.*, Vo+ 316 of Fig. 3, 404 of Fig. 6) **via a discharge common TCCS** (*i.e.*, a TCCS for discharging a TC to said common reference connection, see, *e.g.*, page 13 lines 3-16, and examples - FET 312 of Fig. 3, FET 608 of Fig. 6);

d) **coupling a second opposite terminal** (*e.g.*, right side of 202 of Fig. 3 or 606 of Fig. 6) **of the TC to an output supply connection** (*e.g.*, Vo- 318 of Fig. 3; Vo- 634 of Fig. 6) **opposite the common reference connection via a discharge output TCCS** (*e.g.*, FET 314 of Fig. 3; FET 610 of Fig. 6); **and**

e) **fabricating the discharge output TCCS to have a control node AC impedance** (see, *e.g.*, paragraph 52, page 13 lines 3-16) **at least double a control node AC impedance of the discharge common TCCS.**

V.H Claim 52: Discharging Switch AC Impedance Disparity

A method of generating an output supply (see, *e.g.*, page 7 lines 5-21, page 16 line 27-page 18 line 3, and examples of +/- outputs - 216/218 and/or 224/226 in Fig. 2; 316/318 in Fig. 3; 404/634 in Fig. 6; 404/710 in Fig. 7; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1014/1016 in Fig. 10) **by alternately transferring charge from a voltage source** (see, *e.g.*, page 7 lines 3-12, and +/- source examples - 208/210 of Figs. 2 and 3; 402/404 in Fig. 6; various permutations of Va/Vb, Vd/Vc, Ve/Vf and Vh/Vg in Fig. 9; 1002/common in Fig. 10) **to a transfer capacitor ("TC")** (also called "fly capacitor," see, *e.g.*, page 7 lines 3-12, and examples - 202 in Figs. 2 and 3, 606 in Fig. 6, 902 and 912 in Fig. 9, and 1012 in Fig. 10), **and from the TC to the output supply, the method comprising:**

a) **coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches** (see, *e.g.*, page 12 line 31-page 13 line 7, page 16 line 27-page 17 line 26, and examples - FETs 608 and 610 in Fig. 6; various in Fig. 9; 800 in Fig. 10) **under control of the single phase charge pump clock output** (see, *e.g.*, page 12 lines 27-28, page 14 lines 26-28, and examples - 524 from Fig. 5 for Fig. 6, 802 in Fig. 8 for Figs. 9-10);

b) **coupling the TC to the voltage source via a TC charging switch** (see, *e.g.*, page 12 lines 29-31, and examples - 602 and/or 604 in Fig. 6; devices 800 or devices 830 in Fig. 9; devices 830 in Fig. 10), **during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output;**

c) **coupling a first TC discharging switch** (*e.g.*, 608 of Fig. 6) **in series between a first node of the TC** (*e.g.*, left side of 606 in Fig. 6) **and a common reference connection** (*e.g.*, 404 of Fig. 6) **of the output supply;**

d) **coupling a second TC discharging switch** (*e.g.*, 314 of Fig. 3 or 610 of Fig. 6) **in series between a second node of the TC** (*e.g.*, right side of 202 in Fig. 3; or right side of 606 in Fig. 6) **opposite the first node and a connection of the output supply** (Vo- 318; or Vo- 634 of Fig. 6) **opposite the common reference connection; and**

e) **fabricating the second TC discharging switch to have a control node AC impedance** (see, *e.g.*, paragraph 52, page 13 lines 3-16) **at least twice as large as a control node AC impedance of the first discharging switch.**

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented for review:

Whether Claim 18-19 and 70-71 are unpatentable under 35 USC § 103(a) as obvious over Imamiya in view of Pfiffner.

Whether Claims 1-4, 9-10, 12-14, 16-17, 28-33, 36-41, 43-45, 48, and 68-69 are unpatentable as obvious under 35 USC § 103(a) over Imamiya in view of Ito.

Whether Claims 5-8, 15, 34-35, 46-47 and 54-59 are unpatentable as obvious under 35 USC 103(a) over Imamiya in view of Ito, and further in view of Yamashiro.

Whether Claims 20 and 22-23 are unpatentable as obvious under 35 USC § 103(a) over Imamiya in view of Pfiffner, and further in view of Ito.

Whether Claims 24-25, 27, 60-61 and 66-67 are unpatentable as obvious under 35 USC § 103(a) over Imamiya in view of Yamashiro.

Whether Claims 1-2, 4, 9-10, 12-14, 16-17, 28-33, 36-41, 43-45 and 68-69 are unpatentable as obvious under 35 USC § 103(a) over Forbes in view of Ito.

Whether Claims 1-4, 10, 12, 14, 16, 43-44, 48, 50-51, 53, 57-58 and 68-69 are unpatentable as obvious under 35 USC § 103(a) over Tasdighi in view of Yamauchi.

Whether Claim 49 is unpatentable as obvious under 35 USC § 103(a) over Tasdighi in view of Yamauchi, and further in view of Pfiffner.

Whether Claims 50-51 and 53 are unpatentable as obvious under 35 USC § 103(a) over Imamiya in view of Ito, and further in view of Yamashiro and Clark.

Whether Claims 1-10, 12-17, 20, 28-41 and 68 are unpatentable under 35 USC § 112, second paragraph, as being indefinite.

VII. ARGUMENT

The Appellants regret the extreme length of this Appeal Brief. A restriction requirement of up to four ways was originally expected but not issued; while that is not unreasonable in view of the closely related nature of the claims, it leaves four complete families of claims pending in this Appeal, each family distinguished differently over the prior art of record. Moreover, the Examiner has chosen to reject most claims over a multiplicity of essentially cumulative prior art combinations, rather than to narrow the argument to the most pertinent references. Finally, the legal effect whereby failure to submit an argument waives such argument essentially forces the Appellants to point out each of the significant flaws in the Examiner's rejections. The arithmetical product of the large number of claims, multiplied by the multiplicity of rejections of each, multiplied by the number of flaws in each ground of rejection, has resulted in a daunting matrix of arguments, and a paper that is anything but "brief." Moreover, the sheer volume of issues makes it difficult to set forth arguments just once, and then reference them as needed, so many arguments set forth herein are to some extent redundant.

In view of the complexity and length of this Appeal Brief, an overview of the significant issues has been added, and summaries of the invention and the reasons that the claimed subject matter is nonobvious have also been set forth above. Although very helpful in view of the complexity of the Brief, the overviews and summaries also add to the overall length. The rejections are set forth and addressed in groups according to the particular combination of references relied upon. However, the grounds of rejection make a great deal more sense when considered in view of an understanding of the most significant features of the claimed invention, as well as overarching principles of inventiveness. Moreover, certain errors of examination are repeatedly made, and should be considered so that they can be understood in respect of particular rejections. The summaries should facilitate an understanding of such important claimed features, examination errors, and principles of inventiveness.

VII.A. SUMMARY OF MOST SIGNIFICANT EXAMINATION ISSUES

This section is a summary of issues that are common to a multiplicity of claims. This section also provides an overview of the inventive nature of the claimed subject matter. A number of issues are recharacterized as factual matters in an effort to conform this Appeal to the requirements set forth in *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705; 127 S. Ct. 1727 (2007) . Some of these factual matters are set forth in the following remarks.

In a nutshell, the Appellants deserve patent protection for features that have been previously thought undesirable, and which therefore have not and would not be used, and which can be seen now to be desirable only because of the Appellants' contradiction of the teaching that has been set forth by many scores of highly skilled IC charge pump designers over three decades of IC charge pump prior art development.

VII.A.1 The Fundamental Nature of the Appellants' Discovery

IC charge pumps are used in a substantial fraction of all integrated circuits. IC charge pumps are one of the most crowded fields of electronic design, having been under active development for over thirty years, and having spawned hundreds of patents and papers, of which over 100 are of record. Prior art to the Appellants' claims thus represents the wisdom of large numbers of highly skilled and inventive designers.

VII.A.1.a IC Characteristics

ICs, and particularly CMOS ICs, have particular abilities, strengths and weaknesses, many of which changed very little during thirty years of prior art IC charge pump development. A strength of (especially CMOS) ICs is the digital signal processing they effect with extremely small active devices that consume very little power. This strength has increased over time with improvements in lithography. A weakness of ICs is that capacitors, though irreplaceable for purposes of storing conveying charge and for some other purposes, occupy a great deal of IC area, which means that they are expensive to implement. As such, IC (and especially CMOS IC) circuit designers are obliged to avoid using capacitors except as necessary. IC capacitors have been improved through

better processing techniques, but the improvement has not been as rapid as the improvement in digital circuit density and capability.

VII.A.1.b Consequent IC Charge Pump Design Characteristics

These IC strengths and weaknesses have informed the development of IC charge pumps. It was seen from the earliest days of charge pump design, for example, that capacitive coupling of signals was undesirable because it entailed not only the area penalty of a capacitor, but also biasing circuitry which itself can occupy significant area, especially for high impedances. If lower impedance biasing is employed, then larger capacitors are necessary to couple a signal to a given node without undue signal degradation. As such, it was clearly undesirable in the prior art to use capacitors for coupling signals that could effectively, and much less expensively, be coupled by tiny active circuits. This led designers to reject unnecessary signal-coupling capacitors, even though they were a staple of non-integrated circuit design.

Designers also rejected slow-edged control signals for some of the same reasons. First, fast-edged control signals are easier to couple via active, low-power CMOS circuits. Second, fast-edged control signals are less likely to create timing uncertainty. Third, the fast-edged control signals permit a charge pump transfer capacitor to be either charging or discharging for a larger proportion of the available time than is possible with slow-edged signals. (The extended remarks in this regard are set forth in subsection *VII.A.3.a Integrated Circuit Charge Pump Clock Waveforms* are incorporated here by reference.)

For all these reasons, during the course of over thirty years of development, IC designers, especially those having access to the digital processing capabilities of CMOS, have uniformly avoided employing capacitive coupling when coupling "control only" clock signals to transfer capacitor (TC) charging switches (TCCSs). They have also universally avoided using very slow-edged clocks.

VII.A.1.c Known Charge Pump Problems Have Been Well Solved

For thirty years of active IC charge pump development spanning every conceivable charge pump architecture, these features — fast-edged clock waveforms, and no capacitive coupling of

"control only" clock signals to TCCSs — have remained constant, like the basic characteristics of IC design that underlie them. During the course of this development, all known fundamental problems have been laid to rest, with one glaring exception: the problem of excess noise generated by a charge pump.

VII.A.1.d Charge Pump Noise

Charge pumps have long been known to generate significant noise. The majority of IC charge pump designers were resigned to simply tolerate the noise produced by charge pumps. In some circuits, to be sure, such noise is trivial compared to much worse noise generated by massive high-speed digital switching. However, in sensitive analog circuits noise remains an unsolved problem so serious that it can prevent a circuit from being commercially viable. Such was the situation faced by the Appellants, who required a charge pump that provided bias voltages for a cell phone transmitter power amplifier and antenna switching circuitry. The proximity of the circuitry to an antenna, together with very strict regulatory limits on allowable noise production, threatened to render some circuits a commercial failure. Despite the efforts that had previously been made to limit charge pump noise generation, the conventional wisdom was clearly inadequate to address noise problems faced by the Appellants. Necessity, as is often noted, is the mother of invention.

VII.A.1.e Noise is Unpredictable

The Appellants were obliged to turn their back on the vast conventional wisdom distilled from over thirty years of IC charge pump development. Their problem was particularly difficult because noise is produced to some degree by all operating electronics, but is almost never an intended result. Being unintentionally produced by all components, no analytical method exists to identify the most significant contributors to noise generation. In regard to noise, electronics is as unpredictable as any chemical system.

VII.A.1.f Solving The Noise Problem

Through trial and error, the Appellants eventually developed a circuit that greatly reduced noise generation by an IC charge pump.

VII.A.1.g Identifying Important Aspects of the Solution

Noise reduction is one aspect achieved by limiting high frequency noise by generating a clock waveform having edges as slow as reasonably possible. A balanced current starved ring oscillator was first chosen because the current limiting circuits also minimize noise coupling back into the supply. However, such current limiting alone was insufficient; one important feature was a clock waveform that was much slower than was ever used in the IC charge pump prior art. Having created such a slow clock, the Appellants essentially created a new problem of coupling such clock signals to the switches controlled thereby. If conventional active circuits were employed, it would be difficult to avoid "sharpening" the edges of the clock (raising the "dv/dt" of the clock signal). Consequently, the Appellants turned to a coupling method which, while certainly well understood, had been uniformly rejected by IC charge pump designers who had access to significant digital processing power, such as CMOS IC designers.

VII.A.1.h A Fundamental Discovery, Ignored

The most fundamental aspect of the Appellants inventive design, then, may be seen to be the generation of a slow clock, together with using such slow clock to control the charge pump switches (TCCSs). The causal link between the clock signal and charge pump noise generation is very unexpected, and is so fundamental that it is not believed to have ever been suggested previously. Uncovering it was a very significant advance in a charge pump field that had been relatively static for many years. This discovery by the Appellants is fundamental not only to the charge pump feature combinations that they claim, but also as an advance to the field of IC charge pumps.

In the face of this very fundamental discovery, the Examiner has been impatient for the Appellant to focus on circuit minutiae, stating for example (Office Action reopening prosecution issued May 17, 2007, page 38 lines 12-17):

> Therefore, this examiner strongly believes that for any significant progress with the present application to occur, the applicants should begin to concentrate on specific, novel, technical features of the invention that are clearly supported by the original disclosure and figures, without dwelling into (and maintaining) the use of well known circuits, and numerous variations of their combinations, that one of ordinary skill in the art would also clearly understand.

In keeping with this belief, the Examiner has allowed claims limited to certain minor circuit details. However, such claims do not begin to protect the fundamental invention of the Appellants. Fundamental insights are not often made in fields as well established as IC charge pump design, and the Examiner is either unwilling or unable to recognize or credit them here.

VII.A.1.i Connection Between the Fundamental Discovery and Claimed Subject Matter

Precisely because the underlying insight is fundamental, some connections are obscure: connections between groundbreaking discoveries, such as the advantages of using a slow clock; the problems entailed by such discoveries, such as a need to couple a slow clock without speeding it up or coupling it into the power supplies; and the implemented circuit features that are contrary to all conventional IC charge pump wisdom and that are rendered desirable only by Appellants' discovery.

It is the nature of electronic circuits that building blocks are extremely common: capacitors, resistors, inductors, and a few types of active circuits. These blocks are all "clearly understood" by those of skill in the art. What the Examiner has missed, however, while focusing on circuit minutiae, is the fundamental nature of Appellants' underlying discovery and the way it impacts many aspects of charge pump design in order to render desirable features which, while always possible, were universally rejected. The individual features claimed by the Appellants are "well known" in the sense that the building blocks of electronic circuits are all "well known." However, the feature combinations claimed by the Appellants have been universally rejected in the extensive prior art of charge pumps because common sense and market pressures all pressure the charge pump designer away from these circuits. The circuit features claimed by the Appellants are contrary to the wisdom of over thirty years of IC charge pump development, and would not have been used by those of skill in the art. The only reason to create a design comporting with the Appellants' feature combinations, which is so clearly contrary to extremely well established conventional wisdom, is the Appellants' fundamental insight into the causal relationship between charge pump clock waveform and noise.

The Appellants' fundamental discovery about noise generation has rendered desirable previously unused and rejected circuits, and has provided an important reason to contravene the

conventional wisdom of charge pump design that had been developed for thirty years before the Appellants' discovery and inventions. The subject matter claimed by the Appellants has been rejected by those skilled in the art, and would not have been used if not for their discovery.

VII.A.2 Principles of Nonobviousness Pertinent to Appellants' Claims

The Appellants set out to solve a problem that that was an unintended consequence of charge pump designs, the cause of which was unknown and the solution to which was therefore not predictable or subject to resolution by either straightforward analysis or application of known techniques. It is submitted that the problem associated with circuit noise generation in this context has not been adequately solved before, despite numerous attempts, precisely because the source of the problem identified by the Appellants has not been known. The solution to the problem was entirely unpredictable because the cause was not well understood. No skilled person would have predicted that the features now claimed by the Appellants would help solve the longstanding problem of excessive noise generation.

Far from there being some reason to modify the references as proposed by the Examiner, the proposed modifications were seen as undesirable by persons of skill in the art at the time of the invention. It is only due to the Appellants' discovery of a significant cause of IC charge pump noise that the claimed combinations became worth implementing, rather than economically undesirable or impractical.

The foregoing issues provide context to inform an analysis of factual issues as required by *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), as reaffirmed by *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 715; 127 S. Ct. 1727, 1734 (2007). The factual inquiries require determining the scope and content of the prior art; ascertaining the differences between the prior art and the claims at issue; and resolving the level of ordinary skill in the pertinent art. The Appellants differ with the Examiner as to several of these factual determinations.

An overview of the manner in which these general issues of patentability apply to the claims, and of the disputes between the Examiner and the Appellants in this regard is set forth below.

VII.A.2.a Long Felt Need and Unpredictability of Solution

The electronic arts are generally thought of as predictable. However, complex circuits invariably produce electrical noise as an unintended consequence of operation. The particular sources that contribute to unintended noise radiated by a circuit are never known with certainty. When a particular result is intended, electronics may typically be designed to produce it using empirical, or at least well understood, procedures. But the accidental, or unintended, consequences of a circuit design are, by definition, not known. Noise produced by a circuit is not only a function of a source, but of transmission methods, again unintended, that couple the source to sensitive locales. Consequently, avoiding noise in electronic circuits is not a predictable design skill.

The unpredictability of designing circuits to reduce unintended noise creation should be obvious to all persons having practical experience in mitigating noise in electrical and electronic devices. However, the extensive integrated circuit (IC) charge pump prior art of record indicates that it has long been known that charge pumps have a problem of generating undesirable noise. (The remarks in this regard set forth in subsection *V.A.1 Well Known Noise Problem Has No Satisfactory Predictable Solution* are incorporated here by reference.) Moreover, the IC charge pump prior art includes several references of record that purport to address this problem. The solution set forth in each reference differs wildly from all other solutions. In particular, no IC charge pump prior art reference of record even hints at the noise reduction solutions discovered by the Appellants and described in the subject application.

The noted references indicate that the problem of noise generated by charge pumps has long been recognized. The paucity of references addressing the problem indicates that, for the most part, designers simply tolerate noise generation, or else use different methods to obtain auxiliary supply voltages. Thus, it may fairly be stated both that there is a long-felt but unmet need for quieter charge pumps, and that the design of solutions to the problem are not predictable.

*VII.A.2.b **Sole** Motivation to Modify the Prior Art As Claimed is Appellants' Invention*

Hindsight analysis is initially difficult to avoid when considering claims that are not anticipated by a single prior art reference. However, the roadmap provided by the inventors' claims

was not known at the time of invention, so a reason why a skilled person would have made a particular claimed combination, at the time of the invention, is still needed to find obvious a claim that is not anticipated.

A combination is not obvious merely because it is possible ("That one *could* invent such a cable tie is unquestioned. Caveney *did*. The question, however, is never whether an invention *could* be made, but whether there is anything in the prior art as a whole that would have rendered its making obvious to one skilled in the art when the invention was made." *Panduit Corporation V. Dennison Manufacturing Co.*, 774 F.2d 1082, 1092, 227 U.S.P.Q. 337, 347 (Fed Circuit, 1985)). It must be desirable, and a skilled person should have recognized that it is desirable ("A person having ordinary skill in the art could have combined Asano with a pedal position sensor in a fashion encompassed by claim 4, and would have seen the benefits of doing so." *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 724; 127 S. Ct. 1727, 1743 (2007), emphasis added). Recognition of desirability is one way to describe a motivation to combine.

It is still important to determine a motivation for a particular combination of features in the prior art in order to render obvious a claimed invention ("Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 723; 127 S. Ct. 1727, 1741 (2007), emphasis added). Thus, even though a combination is within the ability of a skilled person, if there is no reason to deviate from the wisdom of a crowded field to make such combination, and there is good reason not to do so, such combination clearly is not obvious.

Prior to the advent of integrated circuits, capacitors were commonly used to solve the problem of coupling a signal to a differing voltage level. In ICs, however, capacitors take up a great deal of IC space. Increased space in an IC translates directly to increased cost. Accordingly, ever

since the advent of ICs, designers have worked hard to find ways to avoid the use of capacitors in ICs. An IC designer would never use a bulky capacitor when solutions requiring only much smaller active devices are well known.

In the field of charge pumps, with respect to claimed features such as substantially sine-like clock outputs, 3-stage CSRO charge pump clock generators, and non-TC capacitive coupling of charge pump clock output to TCCSs, the advantages and disadvantages had not changed significantly in thirty years of prior art development. If anything, the reduction of size of active components in CMOS ICs has rendered the use of capacitive coupling even more undesirable compared to the conventional alternative of coupling via active devices, when wires will not suffice. The reduction in size has also arguably reduced the disadvantage of requiring more stages in a CSRO, while increasing the advantage of using generally square clock signals suitable for active coupling. Thus, the most apparent change in ICs during thirty years of prior art development, a reduction in geometries, tended to make the claimed features less desirable from a conventional standpoint.

The breadth, depth and time span of directly pertinent prior art must have a bearing on obviousness. When directly relevant prior art has developed deeply and broadly over a long period of time, significant deviations from the thoroughly developed wisdom of such prior art must be strong evidence of nonobviousness, unless some recently emerging motivation drives a change that can reasonably be expected to improve an old design in a predictable way. Nothing had changed in the crowded field of charge pumps that would make any of these claimed features, which had previously been universally avoided, suddenly desirable.

What changed, at the time of the invention, was Appellants' unforeseen and unpredictable discovery of **the relationship between charge pump clock output waveform and noise generation by a charge pump.** The Examiner does not suggest that anybody else discovered this relationship. In light of that discovery, and only in light of that discovery, a variety of previously rejected IC designs suddenly were discovered by the Appellants to be desirable. Appellants therefore have applied for patent for these previously unused, undesirable combinations that are desirable only in light of their significant innovative discovery.

The Examiner continually fails to submit any motivation that would lead a skilled person to design an IC charge pump contrary to the thoroughly explored wisdom of charge pump design, which has been accumulated over a period of more than thirty years by the most highly skilled and inventive designers.

The rare example in which the Examiner actually suggests a plausible motivation for a claimed feature actually underscores the persuasive force of the weight of contrary prior art. The Appellants claim a charge pump clock generated from a ring oscillator having not more than three inverter stages, which, on the evidence of record, is less than has been employed in any charge pump prior to the Appellants' invention. The Examiner suggests that the motivation to modify a charge pump of the prior art to have fewer stages rests in the advantage of requiring less parts. The problem with this suggestion is that this same advantage has existed during the entire development period of IC charge pumps, which spans over thirty years; and rather than increasing, this advantage decreases as lithographies become progressively finer. The extremely well developed prior art of charge pumps has developed at all times in the presence of this advantage, and yet all designers have ignored the proposed advantage and have not thought to suggest or disclose a current starved ring oscillator having only three stages. On the principle of *res ipsa loquitur*, the avoidance of such feature by hundreds of skilled designers bespeaks its apparent undesirability. The drawbacks associated with the use of three stage ring oscillators clearly greatly outweigh the apparent, if modest, advantage of reduced parts count, or else some designer would have disclosed such a design.

VII.A.2.c Scope and Content of the Prior Art

The Appellants have less disagreement with the Examiner's assertions as to the content of the prior art, because the Examiner has finally withdrawn many grounds of rejection that were based upon an absence of disclosure, coupled with bald conjecture as to how prior art charge pumps "might" or "could" have been designed. However, the Examiner replaced such failed grounds of rejection with grounds based not on an absence of disclosure, but on actual disclosure from references that are not properly within the scope of prior art that a person of skill in the art would follow or consider when designing charge pumps. Thus, instead of an absence of disclosure, the

Examiner now asserts that a skilled person would turn to nonanalogous prior art, despite the abundance of available analogous prior art that has been proven suitable for use in charge pumps.

Scope of Prior Art that a skilled person would follow: Charge pumps constitute a very crowded field of art. There are 94 references of record. Of these, 83 references of record specifically discuss or apply to an integrated circuit charge pump, and thus may constitute analogous prior art that a skilled person would consider when designing a charge pump. An IDS is submitted herewith that contains 24 additional specifically charge pump references. Thus, extremely numerous pertinent references are available to the skilled person interested in designing charge pumps.

Integrated circuit charge pump patents have filing dates dating back to at least 1972, so they have been actively designed for more than three decades. Because charge pumps are used to provide substrate biasing, as well as for many other purposes, a very substantial fraction of integrated circuits include a charge pump of some type. Clearly, then, charge pump designers had access to a wealth of information that is completely specific to charge pumps. Because skilled inventors had been resolving problems associated with charge pumps for three decades at the time of the present invention, a designer could and would rely on conventional teaching that had been proven suitable for the special requirements of IC charge pumps. It is not inventive to follow the voluminous teaching of charge pump prior art, but it would be inventive to reject the teaching of charge pump prior art in favor of features that are not used anywhere in the extensive prior art of charge pumps. If a feature has not been used in any of the many relevant charge pump references of the prior art, then there must be a compelling reason that such feature has been so thoroughly avoided by IC charge pump designers.

While patent references rarely provide reasons for that which inventors choose not to practice, the absence, after so many decades of development, of features that are certainly known possible to persons of skill in the art is strong circumstantial evidence that such features are considered undesirable. In view of the crowded field of charge pump art, the undesirability implied by an absence of the claimed features properly overcomes the Examiner's conclusory assertion that modifications to charge pumps would obviously be made according to nonanalogous prior art

elements. This is especially true because the Examiner suggests no motivation for making such modification other than that "it could be done."

While the Examiner fails to carry the burden of showing any motivation for a skilled designer to modify a charge pump contrary to the extensive teaching directed expressly to charge pumps, the Appellants not only rely upon the implication of the absence in the analogous prior art of the claimed feature combinations, but go farther to demonstrate motivations that would discourage a skilled person from deviating from the charge pump teaching.

Thus, the scope of the prior art that a skilled person would follow is really a matter of motivation. A skilled but conservative charge pump designer will follow teaching that he has reason to believe will work suitably for charge pumps because it is expressly disclosed for use with charge pumps. An inventive designer, trying to solve a long-standing problem that the prior art has failed to address, will indeed look elsewhere. But there is no problem, such as the known one of excess noise, or other motivation such as market advantages, that would motivate a skilled person to deviate from the teaching of the analogous prior art in the manner claimed by the Appellant.

The connection between the feature combinations claimed by the Appellants, and the underlying invention of the Appellants, is so obscure that the Examiner frequently and plaintively demands to know what, exactly, the Appellants think of as their invention. The Examiner's exasperation is actually strong evidence that one of skill in the art would not obviously choose to make the claimed modifications to solve the problem of noise. Reducing noise by substantially slowing the clock is the underlying invention, which is difficult to claim but leads to particular feature combinations that are undesirable except in view of the Appellants underlying invention. So the Appellants' underlying, unifying inventive concept provides the motivation for feature combinations that would not otherwise be made by persons of skill in the art.

The properly analogous prior art is that prior art that a skilled person designing a charge pump would follow if he had no motivation, other than those found in the prior art, to deviate from decades of charge pump development. That analogous prior art is properly limited to prior art that expressly recommends features suitable for use in charge pumps. In other words, the proper scope

of prior art that a skilled person would follow, in view of the extremely crowded nature of this field, is the charge pump prior art.

This is particularly true for the central features pertinent to charge pumps, such as the clock waveforms and timing, and the interactions between the clock(s) and the transfer capacitor charging switches (TCCSs). The specific requirements of charge pumps restrict choices in respect of such parameters. Some aspects of charge pump designs, such as the type of integrated circuit process employed, may affect the scope of prior art that would be considered. For example, GaAs ICs cannot readily employ complementary (N- and P- channel) MOS devices. As such, GaAs IC designs may have to include features that would not be used in CMOS ICs, because CMOS ICs have much greater design flexibility using tiny active devices.

When designing a passenger automobile, a designer needs to select or design an engine. Even though they are well known, an automobile designer would not consider employing a jet engine, or an engine designed as an outboard motor for a boat, because numerous designs exist that are already known to be suitable for automobiles, and which are expected to be much less expensive than jet or outboard motor engine modifications. The proper scope of prior art that an automobile designer might reasonably be expected to consider would thus not include jet engine or outboard motor prior art.

Just as an automobile employs an engine but has special requirements that limit the range of engines a skilled designer would consider, charge pumps employ an oscillator. However, while oscillators are made for many purposes and thus may have outputs that are square, sinusoidal, triangular, or even more exotic, oscillators that are actually suitable for charge pumps have been selected for prior art charge pumps. A skilled IC charge pump designer would not just whimsically modify a charge pump by replacing the oscillator with one that has never been used in IC charge pumps before, unless he had some compelling reason to do so. Thus, the charge pump prior art does not reasonably extend to encompass oscillators that are not expressly disclosed for use in charge pumps.

Charge pumps necessarily use capacitors, and while capacitors of sufficient size were once so difficult to fabricate that they were often not fabricated on the integrated circuit itself, there is a

strong advantage to avoiding such off-board connections. As such, capacitors that are unavoidable for charge pump operation, such as charge transfer and filtering capacitors, are now most often fabricated on the integrated circuit chip. However, capacitors still take up far more IC chip area than numerous low-power active devices, particularly in the case of CMOS ICs. While a CMOS IC designer knows how to use capacitors, he would not do so when the prior art of charge pumps clearly shows alternatives that require only a few small active devices, rather than large capacitors. Barring some compelling reason, a skilled designer would look to charge pump prior art to see what functions could be effected inexpensively according to an IC process, and when the designer should instead resort to the use of capacitors. The same general principle applies, that in a wealth of directly applicable prior art, a skilled designer would be unwise to randomly modify designs in a manner contrary to three decades of research and development of prior art charge pumps.

Claim features that are not taught or suggested in the appropriate prior art are described briefly in the remarks set forth below.

VII.A.3 Inventive Nature of the Most Unique Claim Features

Each claimed invention is a charge pump, and the inventive concept that ties together the primary features is their ability to facilitate the generation and/or coupling of a "slow" charge pump clock to the switches controlled thereby. A skilled person would not incorporate these claim features into integrated circuit (IC) charge pumps, especially CMOS IC charge pumps, except to permit the advantages of a slow, analog charge pump clock waveform, as taught by the Appellants.

VII.A.3.a Integrated Circuit Charge Pump Clock Waveforms

The reason that computer signals are almost universally binary is that integrated circuits (ICs), especially CMOS ICs, can far more efficiently deal with two-state information and waveforms than with signals that vary continuously over an infinite number of states. Binary waveforms are easier to create, easier to propagate and easier to manipulate. Active devices that implement such propagation and manipulation of binary signals can be extremely small. Power supplies generally need to include some analog aspects; however, insofar as possible, it is far more space efficient to perform functions that are suitable for binary treatment using binary techniques.

Analog computation is known to be possible, yet processing digital or binary information is so much more efficient that most computation involving continuous, analog waveforms is performed by first converting the analog waveform to digital, processing the resulting information digitally, and reconfiguring the processed information into a resultant analog signal. Two non-trivial extra steps of conversion between analog and digital forms of the information are rendered worthwhile due to the greater efficiency of digital processing versus analog signal manipulation.

A binary clock signal is thus desirable in ICs (especially CMOS ICs) because it is more easily generated, more easily modified, more easily controlled, and more easily coupled. Easy control of the timing of a digital signal simplifies the avoidance of damaging (and noisy) simultaneous conduction spikes through transfer capacitor conduction switches (TCCSs), as is remarked upon elsewhere in this Brief. TCCSs are generally only reliably fully conductive, or reliably fully non-conductive, toward the extremes of the control voltages applied to them. The fly capacitor is charged only during a "charge" time at one end of a control voltage (clock) swing, and is discharged only at the other end of the clock swing. If the clock is square, full charging occupies nearly 50% of the available time, and full discharging occupies nearly the other 50% of the available time. To the extent that the clock is not square, the charge and discharge times are reduced as a proportion of the cycle time. As such, a slow clock will generally require increased rms charge and discharge currents to make up for substantial non-conduction time.

The analysis of prior art waveforms in subsection *VII.B.10 Supporting Remarks: Analysis of Clock Waveforms in Prior Art of Record* provides additional evidence in support of the foregoing remarks.

VII.A.3.b Coupling IC Charge Pump Clock to TC Coupling Switches

There are circumstances in integrated circuits when a capacitor is desirable in an IC, despite its large size and "cost" in area. As examples, capacitors are indispensable when charge must be stored for a voltage supply, or pumped from one supply to another in a charge pump. But in order to efficiently fabricate charge pumps on integrated circuits, designers use no more capacitors than are required. Indeed, the earliest IC charge pumps are believed to have included no capacitors on the IC, all of the input, output and transfer capacitors instead being external to the IC. To make processing

suitable for an IC, the clock signal was made square or pulsed, so that it could be coupled as needed using only simple, tiny active devices. Space-consuming capacitors were avoided, as may be seen in the relevant prior art.

Capacitors may sometimes be useful when coupling a complex analog waveform to a target at a different voltage level, which otherwise requires somewhat complex, and less power efficient, operational amplifier circuitry, rather than merely simple digital gates. However, they are not needed to process binary information, which can readily be processed using logic gates. Digital processing is so much simpler that most analog information is converted into digital signals that are processed digitally and then reconverted back to analog signals, if that is necessary to drive an analog transducer such as a speaker.

Thus, both capacitors and analog signal processing have been actively avoided in charge pump designs. Designers did not desire slow, analog charge pump clock waveforms prior to the Appellants' invention; and even when a clock generator was permitted to be less than square, the designer would not expend effort to maintain such a slow clock waveform, but instead would couple such a clock via active devices, each of which would increase the speed of the edges of the clock signal. The remarks set forth, or incorporated by reference, in subsection *VII.B.10 Supporting Remarks: Analysis of Clock Waveforms in Prior Art of Record* are incorporated here by reference to support and elaborate upon these contentions.

Creating and coupling analog signals is difficult in ICs, requiring either complex amplifier circuitry or a space-consuming capacitor. It is precisely for this reason that modern electronics convert most of the analog information into digital signals for efficient processing.

Capacitors certainly have their place in IC design. However, capacitors are undesirable for use in circuits in which the function for which they are considered, *e.g.*, coupling a clock signal to a switch, can be performed at lower cost by well known alternatives. Despite the fact that none yet have done so, a charge pump designer might use such feature combinations contrary to established practice if they were motivated to do so. However, no such motivation to contravene the conventional wisdom of charge pumps is identified by the Examiner or otherwise seen, with the

exception of the benefits taught by the Appellants in their application - information that was not publicly available at the time of the invention.

VII.A.3.c No Motivation to Modify Charge Pumps Contrary to Decades of Convention

In *KSR*, "market pressures" motivated the use of a digital sensor to input the gas pedal position to the automobile's computer system. The digital sensor did just what it was expected to do: it created the digitized gas pedal signals needed by modern cars; and its use was motivated by market pressures to obtain flexible, inexpensive digitized gas pedal signals. Accordingly, it was deemed obvious. "When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103." *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 723; 127 S. Ct. 1727, 1741 (2007).

In IC charge pumps, market pressures strongly motivate designers to avoid using capacitors to couple the clock signal to transfer capacitor switches. Nor is there a design need to use capacitors for coupling the prior art clock signals, when the coupling device is not also a charge transfer device and therefore necessarily a capacitor, because a combination of direct connection and active circuit coupling is both more powerful and much less expensive. Market forces similarly motivate designers to avoid using slow, analog clock waveforms, due in part to the difficulty of coupling such signals. Market forces dictate the use of active devices to couple clock signals to at least some of their targets, such that the coupling motivated by market forces is not passive and increases the rate of change of voltage of the clock waveform. There is no market pressure to modify conventional charge pumps to conform to any of the feature combinations claimed by the Appellants. The lack of market pressure, or any other motivation, to implement the feature combinations claimed by the Appellants is readily deduced by the fact that the individual elements of the claimed combinations have been available for substantially all of the three decades that integrated circuit charge pumps were being designed prior to the Appellants' invention.

The Supreme Court has addressed motivation in *KSR* (underlining added for emphasis):

> Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 723; 127 S. Ct. 1727, 1741 (2007).
>
> In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under §103. One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims. *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 723; 127 S. Ct. 1727, 1741 (2007)

KSR thus makes clear that the motivation for combining prior art in the manner claimed need not match the motivation driving the claimed invention, and the problem solved may be different. Yet there must still be some problem solved, or some motivation, to render obvious a claimed combination. No known problem exists in the prior art of IC charge pumps that has not been solved dozens of times in the CMOS IC prior art of record, always by means that were different from the distinguishing features claimed by the Appellants. In particular, coupling the clock signal to TCCSs (when not coupling charge) has always, over the decades of charge pump CMOS IC designs, been effected by flexible, tiny active devices, and never by capacitors. Thus, coupling the clock signal to transfer capacitor switches is a problem that has been thoroughly, consistently and satisfactorily solved using tiny, inexpensive active devices.

With no motivation to use capacitive coupling as claimed, and with strong motivation not to do so, a designer of a CMOS IC charge pump would not use capacitors for coupling as described and claimed. Evidence of this fact is apparent from the absolute absence of any such design in the prior art that has been considered, including in the roughly eighty CMOS IC charge pump patents that are of record, and which have been developed by the most highly skilled designers in this field.

VII.A.3.d Benefit of Novel Features is Unpredictable and Obscure

Noise reduction is always unpredictable, but it was particularly unpredictable that using capacitors to couple the clock signal to the transfer capacitor switches would result in a quieter charge pump. Using capacitors for clock coupling in an IC charge pump makes sense only because the Appellants realized that making the clock output a slower, analog waveform, and coupling it in that form to drive switches in the charge pump, would reduce noise. It did not make sense prior to this insight as taught by the Appellants.

The field of charge pumps is extremely crowded; scores of charge pump designs have been found sufficiently inventive to warrant patent protection. Capacitively coupling the clock signal to transfer capacitor switches has been possible, indeed within the ability of those skilled in the art, for the entire period of over three decades that IC charge pump prior art was actively developed. That this option has never been disclosed in a CMOS IC charge pump prior art reference (so far as represented by the extensive list of such references that is presently of record) in those three decades is very strong evidence supporting a conclusion that capacitively coupling the clock signal to IC charge pump switches is unambiguously inferior to the alternatives for such coupling that are available to CMOS IC designers. To designers lacking the Appellants' insight in respect of charge pump noise generation, capacitively coupling the clock signal remains undesirable. The Appellants have solved a known problem in an unexpected way, radically changing basic assumptions about charge pump design, and thereby have found a reason to do what prior art designers always could have done, but would not have done.

Indeed, what has escaped the Examiner in his zeal to reject the Appellants' claims is that the Appellants have *radically changed* basic assumptions about charge pump design. For three decades IC charge pump designers had used square or nearly square clock waveforms, and had uniformly avoided circuits that do not provide a sufficiently square waveform. The Appellants have turned on its head the "wisdom" of the scores of highly skilled designers that developed the prior art of charge pumps over the course of three decades. It is only because of this radically changed assumption about the charge pump clock waveform that capacitive coupling becomes, unexpectedly, desirable despite its cost.

There is a significant cost penalty associated with the design claimed by the Appellants. However, the cost penalty is less significant than the fact that previous devices were simply too noisy to work in their intended application. For designers that can live with the noise generated by conventional IC charge pumps, there remains no reason to use the features claimed by the Appellants. If designers must reduce IC charge pump noise to produce a product that satisfies regulatory requirements, however, the Appellants have provided a solution. It costs more to fabricate, but it works. The Appellants deserve patent protection for the claimed features, which have not been and would not be used by persons skilled in this art except in view of the Appellants' brilliant insight into solving a long-standing problem of excessive noise generated by IC charge pumps.

Electrical noise is an unintended, undesirable (parasitic) effect of every functioning electronic circuit to a degree that is difficult to accurately determine and predict. Because noise is unintentionally produced by many different sources, design alternatives that will significantly reduce noise are almost never predictable by practical analytic means. The problem of noise in charge pump circuits has long been recognized, and some attempts have been made, with very limited success, to alleviate the problem. Of the half dozen or so inventive designers that have addressed this issue in regard to charge pumps, not one has considered the approach taken by the Appellants. Nor has the approach taken by the Appellants been implemented by any other designer of charge pumps, according to the extensive examples of designs by inventive designers of record in the subject Appeal. The nature of the approach taken by the Appellants but no previous designers is described in further remarks set forth below.

All charge pumps have some form of a repetitive clock signal that controls the switching of devices. These switched devices guide charge into a transfer capacitor from a source supply. The repetitive clock signal also controls the switching of devices that guide the charge from the transfer capacitor to an output supply. Thus, a clock is a fundamental part of substantially all charge pump designs. In their efforts to tame the troublesome noise inherent to charge pumps, inventive designers have modified different aspects charge pumps, including aspects of the functioning of the clock. However, no known previous charge pump designer, whether in attempts to reduce noise generation

or for any other reasons, has considered radically changing the shape of the clock waveform from that which has been used in charge pumps since their inception decades ago.

This was true until the Appellants radically changed the shape of the clock waveform as compared to the prior art of record. In view of the extensive searches of the literature performed by the Examiner, and by the Appellants and their representative, the absence of a teaching of this approach in any of the prior art of record is believed to fairly indicate that such an approach simply has not been taken before. The question may fairly be asked as to why the claims have not been allowed in view of Appellants innovation.

One possible answer is it is not easy to claim "a charge pump having a radically different clock waveform." The Appellants claim a clock waveform that is "substantially sine-like," which the Examiner rejects only (and improperly) as indefinite. But overcoming such rejection would not end the difficulty, because only some embodiments of the Appellants' quiet charge pump need have a clock that is "substantially sine-like;" the clock waveform can differ substantially from a sine shape and still be suitably slower than those previously considered acceptable. Though the clock waveform does differ significantly from prior art clocks, it is difficult to define how it differs. It is "slowed down," but that is a relative description that is not a proper basis for a patent claim. Thus, it may be seen that although the Appellants have radically changed an important aspect of charge pumps, yet that difference does not readily lend itself to definition in a manner that encompasses the scope of the Appellants' invention.

Fortunately for Appellants, structural differences over the prior art exist in the Appellants' preferred embodiments that follow from the radical change in clock waveform. These features are absent from the extensive IC charge pump prior art (at least of record) precisely because they are unsuitable for IC charge pumps as conceived in the prior art. Because each such defining feature is disadvantageous in charge pumps designed according to previous approaches, there is, of course, no motivation, in the prior art, to incorporate those features into IC charge pumps. The features comprise known electronic components, but they have always been found undesirable for use in IC charge pumps.

VII.A.3.e Distinguishing Features Contrary to Three Decades of Relevant IC Charge Pump Art

In considering the distinguishing features that involve a charge pump clock or connection of the output of the clock to a transfer capacitor coupling switch (TCCS), the two types of charge pumps described in the remarks set forth in subsection *V.D.1 Two Types of Charge Pumps*, including "direct TC drive" and "control only" charge pumps, should be kept in mind, and are therefore incorporated here by reference.

One distinguishing feature is a ring oscillator configured to create a slow, smooth clock output, contrary to the nearly square outputs of IC charge pump prior art. Oscillators that create nearly perfect sine waves have, of course, been known for many decades. However, oscillators are not used in prior art IC charge pumps. Oscillators are not used in prior art in charge pumps because digital clock signals are easier to produce in an IC, easier to couple and level shift in an IC, and easier to control as to timing within an IC. So uncomfortable are IC charge pump designers with sine-like waveforms that the prior art contains not a single example. In fact, the IC charge pump prior art specifically suggests that ring oscillators should not have too few inverter stages. All possible sizes of ring oscillators are known, but not all have been considered as being suitable for use in IC charge pumps. The fact is that the smaller the number of inverter stages, the less square is the resulting clock signal. This is considered disadvantageous by IC charge pump designers who wish to digitally control the switching devices, *i.e.*, all previous IC charge pump designers. In any event, no prior art IC charge pump (of record) employs ring oscillators having **less than five** inverter stages in the ring, and at least one expressly recommends that not less than five be used.

The ease of producing, controlling and level shifting digital signals adequately explains the fact that prior art integrated circuit charge pumps exclusively use digital means to couple charge pump clocks to (transfer capacitor) switching devices. Moreover, however, capacitors consume far more IC real estate than do digital devices. For those reasons, capacitive coupling of clock signals to "transfer capacitors switching devices" has been avoided in IC charge pumps, and is not found in the voluminous prior art spanning decades of development. Indeed, due to the different voltage levels at which the "transfer capacitor switching devices" must operate, it invariably dictates that simple passive coupling is impractical because passive coupling causes simultaneous conduction of

switching devices that are in series. This is a condition which at the least reduces efficiency and exacerbates noise, and at the worst, destroys devices.

Thus, each of the features that are desirable in embodiments of the Appellants' claimed invention has been found undesirable in prior art IC charge pumps for decades. Yet each of the constituent basic electronic elements of such features, and even subcombinations of such elements, naturally exist somewhere in the prior art of all electronics. For example, oscillators that produce sine waves are common; ring oscillators having less than five inverters may be found; capacitively coupled signals may be found, and certainly passively coupled signals may be found. If the Examiner is not constrained to explain why these features would be combined with prior art charge pumps that are devoid of these features, it is very simple and easy to make a conclusory assertion that such combination of features is "obvious." If thus unconstrained, he may select features, such as coupling capacitors, from the prior art, and, using the Appellants' claims as a roadmap, baldly assert that combining them as taught and claimed by the Appellants is obvious, despite the fact that over three decades of IC charge pump prior art fails to reveal such a combination. This, of course, is the very essence of improper hindsight, cobbling together a colorable rejection by identifying the features listed by the Appellants' claims. It is respectfully submitted that the Examiner fails to make even a reasonable effort to provide a reason or motivation for making the significant modifications taught by Appellants to the established practices of charge pump design.

The absence of any motivation for the combinations that the Examiner sets forth to support the rejections of the Appellants' claims is particularly unfair here, because quelling noise in a circuit is so unpredictable that many designers refer to noise reduction as a "black art." The Examiner's frequently stated position is that there was nothing preventing a designer from creating charge pumps as they are claimed by the Appellants. This is, of course, true or else the Appellants would have been unable in reality to make such combinations. Thus, the Examiner seeks to place an impossible burden on the Appellants to prove that a particular combination could not have been made in the prior art. At the least, this position improperly places the burden on the Appellant to prove that a combination would not have been made, rather than on himself to provide evidence that one of skill in the art would have reason or motivation to create such combination. While the Appellants attempt to demonstrate the absence of motivation, they also protest that the Examiner has

not, in many instances, carried his burden of demonstrating motivation. A failure to provide motivation for a particular combination should especially be found to invalidate the Examiner's assertion of obviousness when the claimed combination is not found, despite the availability of a large body of teaching in respect of prior art IC charge pumps that was developed by highly skilled designers over a period of more than three decades preceding the date of Appellants' invention. The availability of so much teaching of "how to" design a charge pump means that a charge pump designer is unlikely to have a reason to deviate from the conventions of charge pumps as designed by the experts, thus making it particularly inappropriate to simply assume that motivation exists to deviate from such teaching.

Hence we arrive at this Appeal. In order to solve the well-known but unpredictable and inadequately solved problem of noise, the Appellants' have virtually reversed the teaching of all previous IC charge pump designers in regard to the clock waveform. It is, in fact, one of the great about-faces in the (extensive) history of charge pumps. The fact that nothing they have done is impossible should not suffice to preclude them from obtaining a patent having a scope commensurate to their inventive new approach. Over many decades, while such alternatives were always possible, highly skilled designers did not, and would not, design charge pumps as now required by the Appellants.

KSR reaffirmed that obviousness depends on a factual inquiry made in accordance with *Graham v. John Deere* (*KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 715; 127 S. Ct. 1727, 1734 (2007). Remarks set forth below will support the Appellants' contentions that (1) the scope of the prior art must fairly be limited to the large and well-developed body of circuits that are actually employed in an integrated circuit charge pump design; (2) each of the Appellants' claims includes one or more features that is not found at all in the prior art of charge pumps; and (3), even though skilled designers have empirical methods enabling them to design circuits with intended outputs, no such empirical methods are available to avoid noise production, which is never an intended output. Being an unintended byproduct of many sources, the effects of circuit changes on noise production are highly unpredictable.

Remarks set forth thereafter address the four most important distinguishing features claimed by the Appellants. As to three of these, it will be shown that not only was it possible to combine the features as claimed by the Appellants, it has been possible for decades. However, each of the features had predictable disadvantages, but no predictable advantages. Only the extremely novel approach taken by the Appellants renders these features desirable for charge pumps. The crowding of the field of charge pumps, together with the ready availability of the features but their absolute absence in charge pump prior art, support a contention that the known disadvantages strongly outweighed any known advantages.

VII.A.4 Examination Errors Systematically Repeated by Examiner

These errors are systematic, as opposed to mere inadvertent mistakes or simple differences of claim construction or arguable factual disagreements. The Appellants have in most instances been protesting these errors for literally years.

VII.A.4.a Ignoring Contrary Evidence

MPEP 2143.01 includes a bold, capitalized subheading stating "Where the teachings of the prior art conflict, the examiner must weigh the suggestive power of each reference," citing *In re Young*. A similar proposition, that contrary evidence in the prior art as a whole must be considered, is supported in this Brief by *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert denied*, 469 U.S. 851 (1984). *W.L.Gore* is relied upon because the facts in that case are closely analogous to some of the rejections in this Appeal, as described in detail in, *e.g.*, subsection *VII.B.2.c W.L.Gore Compared to Rejections Over Imamiya / Ito and Forbes / Ito*. *W.L.Gore* requires consideration of contrary evidence, especially when significant positive evidence is lacking ("Markwood's rapid stretching of conventional plastic polypropylene with reduced crystallinity would not suggest rapid stretching of highly crystalline PTFE, in light of teachings in the art that PTFE should be stretched slowly." *W.L.Gore* at 1551, emphasis added). That requirement is clearly in accordance with MPEP 2143.01. Despite an absence of clear evidence of required features, the Examiner consistently fails to consider contrary evidence indicating that such features are not fairly taught by the prior art.

As a first example, Independent Claims 1 and 43 each include a limitation requiring a ring oscillator having not more than three driver sections (stages). Three grounds of rejection are outstanding for these claims. For the three-section ring oscillator, one ground relies on Yamauchi, a second on Hara, and the third on Ito. None of these references discloses the required limitation. Tasdighi has no information at all about specifics of ring oscillators. Yamauchi describes ring oscillators for a charge pump having an "odd number" of stages, and moreover represents such ring oscillators with illustrations that actually include only 3 driver sections (Figs. 6 and 7). However, the illustrations break the connections between stages, "joining" the connection lines by three spaced dots " • • • " that is well known to represent repetitive material that has been omitted (typically to avoid cluttering the drawing with redundant detail). Accordingly, these figures cannot be fairly construed as a suggestion that no more than three sections should be used in a current starved ring oscillator for a charge pump.

Ito describes ring oscillators for Voltage Controlled Oscillators, not for charge pumps. Different waveforms are useful for different purposes, and the Appellants acknowledge that three stage current starved ring oscillators are known for other purposes, but contend that such oscillators would not have been used to drive an IC charge pump according to the conventional wisdom of such charge pumps.

The evidence that IC charge pump designers would not employ a three stage current starved ring oscillator is not ambiguous in view of at least two facts. The first fact is that in the crowded field of charge pumps, neither an example of a three stage current starved ring oscillator, nor a suggestion that three is a desirable upper limit for the number of inverter stages of such oscillators, is seen in respect of charge pumps despite extensive prior art and arduous searching. The second, and even more crucial, fact is that Hara teaches explicitly that current starved ring oscillators for charge pumps should have at least five sections (see col. 5 lines 60-62). These two facts are contrary to the contentions of the Examiner, and buttress a conclusion that the prior art does <u>not</u> teach the use of three stage current starved ring oscillators, as required, for use with charge pumps.

As a second example, independent Claim 18 is rejected as anticipated by Tasdighi, while independent Claim 49 is rejected over Tasdighi in view of Ito, and again in view of Yamauchi. Both

claims require a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of [each charging switch and each discharging switch]. In each case, the Examiner relies upon Tasdighi for disclosure of the noted requirement. As noted above, Tasdighi lacks the details relied upon by the Examiner; the evidence is not merely ambiguous, it is entirely absent. Worse, Tasdighi incorporates by reference a further patent, US 4897774 to Bingham et al. ("Bingham '774," *see* col. 3 line 44 - col. 4 line 16), identifying it as the basis for Fig. 4. Bingham shows circuit details that are omitted in Tasdighi. The details revealed in Bingham demonstrate that the source of the illustrations in Tasdighi was contrary to the claimed feature. In particular, Bingham shows that the actual system uses a plural-phase clock and active coupling to the charging and discharging switches. Thus, the Examiner's conjecture as to the circuit that Tasdighi "could have" used is not only wholly unsupported by evidence, it is moreover contrary to the evidence.

In each example, evidence in support of the Examiner's assertion is, at the most, ambiguous, and in each example any remaining question is properly resolved in favor of allowability by proper consideration of evidence that is contrary to the Examiner's assertion. As such, each rejection of independent Claims 1, 43, 18 and 49, as well as all depending therefrom, should be promptly reversed.

VII.A.4.b Refusal to Credit Plain Meaning of a Claim Term

A claim term must be construed in accordance with its plain meaning, unless the Appellants clearly indicate a contrary intent ("In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art." *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298, 67 USPQ2d 1132, 1136 (Fed. Cir. 2003).)

Independent Claims 12 and 28, all claims depending therefrom, and various other dependent claims, all require charge pump clock output that is "substantially sine-like" [due to active limiting circuitry]. The Examiner points to no evidence that the prior art teaches a charge pump clock output that is even *remotely* sine-like. To the contrary, all of the numerous references of record are shown to have square or near-square waveforms. A "sine" has a precisely defined mathematical shape, and

thus "substantially sine-like" is a waveform which, while not precisely a sine, nonetheless is at least generally like a sine, which is clearly different from all prior art of record. The Examiner refuses to credit the plain meaning of the term "sine," suggesting that any alternating waveform could be called "substantially sine-like." By its plain meaning, the claim term merely provides some slight variation around a precisely defined waveform, and is thus readily understood by those of skill in the electronics arts.

The Examiner has rejected these claims as indefinite, an understandable rejection that is addressed in the subsections *VII.C.2.c Rejection of Claims 12-17, 20 and 29-41 as Indefinite* and *VII.C.1 Meaning of the phrase "Substantially Sine-like"*. However, for purposes of obviousness the Examiner is obliged to grant the terms their plain meaning (see MPEP 2111, particularly MPEP 2111.01). Claim words must be given their broadest reasonable interpretation, but there is nothing reasonable about the Examiner's assertion that any alternating waveform that is not a perfect square wave can therefore be considered "substantially sine-like."

MPEP 2173.06 addresses the precise problem of claim terms considered to be indefinite. It states that if the degree of uncertainty is great, then a rejection over the prior art is improper, stating as follows:

> As stated in *In re Steele*, 305 F. 2d 859, 134 USPQ 292 (CCPA 1962), a rejection under 35 U.S.C. 103 should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims.

Thus, if the Examiner is unable to reasonably construe the term, rejections over the prior art are improper. MPEP 2173.06 states that rejections over the prior art are helpful "where the degree of uncertainty is not great."

In the case of the phrase "substantially sine-like," the terms should be abundantly familiar to any person having a passing knowledge of electrical engineering, and thus, "the uncertainty is not great." However, the Examiner has chosen to disregard the plain meaning of the terms and instead construe it in an extraordinarily overbroad manner, consequently wasting his own efforts setting forth numerous grounds of rejection based on "considerable speculation about the meaning of terms"

and therefore improper, which the Appellants and now the panel are obliged to consider and address.

VII.A.4.c Omission of Motivation for Modifications Contrary to Conventional Wisdom

The Appellants' discovery that the waveform of the drive signal for the TC coupling switches can cause undesirable noise generation by a charge pump is remarkably new and different in a mature and crowded field. This discovery renders desirable a number of features previously held so undesirable that they have never, so far as the evidence indicates, been employed in thirty years of particularly CMOS IC charge pump development. The Appellants' discovery provides a novel motivation that has previously been absent from the conventional wisdom.

It is for this reason that it is a crucial mistake for the Examiner to fail to identify a motivation to make the changes to the prior art that are required by the Appellants' claims. In electronics, once a thing is chosen to be done, doing it is generally "obvious." However, there must be a reason to make changes to the conventional wisdom developed over the course of thirty years by scores of talented designers.

For each distinguishing feature required in the Appellants' claims, the Examiner seems to assume that because the feature is performing a task, therefore the task was a problem and the feature is a solution to that problem. As a concrete example, the Appellants claim capacitive coupling of a clock to a switch under certain restricted circumstances. The Examiner's reasoning implies that he believes that "coupling a signal" is a problem, and is rather mystified that the Appellants have the temerity to claim that their solution to this problem is novel and nonobvious, when it is clear that capacitive coupling is well known as one of many possible solutions to the problem of coupling a signal.

The error here is in the Examiner's assumption about the nature of the problem solved by the Appellants. As is apparent from the title as well as the content of the subject application, the problem that the Appellants are solving is excessive noise generation by a charge pump. Unlike a need for coupling, for which entirely satisfactory solutions are well known, the problem of noise is not well understood, and has never been satisfactorily solved.

There was no new problem, and no existing problem, of coupling in the prior art. Skilled and inventive designers had provided coupling circuits so suitable that they were found desirable by virtually all CMOS IC charge pump designers for the entire thirty-plus years of prior art IC charge pump development. Over that period, the disadvantages of capacitive coupling (as claimed) were so clear that every single CMOS IC designer avoided such capacitive coupling.

Only the new coupling problem resulting from the Appellants' discovery required a change to the well-established conventional wisdom about coupling the clock to the switches. The Appellants discovered an unexpected relationship between the drive signals to the transfer capacitor (TC) charging switches (TCCSs) and noise generated by the charge pump. They discovered, contrary to the practice of three decades of charge pump wisdom, that slow-edged clock signals helped reduce noise, as did using such slow signals to drive the TCCSs.

By virtue of their discovery, the Appellants have generated a new problem, because the conventional active circuit solution for coupling the clock to the TCCSs in a charge pump can only with difficulty couple a slow analog signal, particularly without causing increases in the dv/dt of the clock signal before it reaches a TCCS. But while the Appellants' discovery creates a new problem that motivates changes to the conventional wisdom of charge pump design, that motivation and problem was not known to those skilled in the art at the time of the Appellants' invention.

Although asserting that "Rigid preventative rules that deny factfinders recourse to common sense [...] are neither necessary under our case law nor consistent with it," the Supreme Court was careful to point out that "A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. See *Graham*, 383 U. S., at 36 (warning against a "temptation to read into the prior art the teachings of the invention in issue" and instructing courts to " 'guard against slipping into the use of hindsight' " (quoting *Monroe Auto Equipment Co.* v. *Heckethorn Mfg. & Supply Co.*, 332 F. 2d 406, 412 (CA6 1964))). *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 724; 127 S. Ct. 1727, 1742 (2007). Aside from the discovery by the Appellants, there simply was no reason at the time of the invention to contradict the conventional wisdom of IC charge pump design established over the course of more than thirty years of IC charge pump development.

The Appellants do not question that other motivations to make the claimed modifications to the prior art of charge pumps may be proper. "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims." *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 723; 127 S. Ct. 1727, 1742 (2007).

However, no such known problem existed prior to the Appellants' discovery. Aside from the issue of noise, there was no problem with charge pumps that was not amply solved over the course of more than thirty years of development. During that development, IC designers found desirable techniques for coupling the clock to the TCCSs, and the chosen techniques remained perfectly satisfactory for conventional charge pumps at the time of the invention. Not only did no problem exist, reasons not to couple the signals as claimed by the Appellants were well known: capacitive coupling requires significantly more area on a CMOS IC than the few active components needed to couple the clock digitally, and moreover required corresponding biasing circuits. In view of the digital processing capability of IC circuitry, and especially of CMOS IC circuitry, such coupling has uniformly been implemented by means of active circuitry. Never, so far as the art of record indicates, has a CMOS IC designer found capacitive coupling of such signal to be desirable, except when the coupling capacitor actually transfers charge to the output, serving as a transfer capacitor, and therefore necessarily a capacitor.

The issue of coupling a clock to control switching circuits in a charge pump has been long and thoroughly solved. The solutions employed during thirty years of CMOS IC charge pump design have not included the solution now claimed by the Appellants. Instead, the prior art of charge pumps has long rejected the coupling method now claimed by the Appellants.

Coupling as claimed by the Appellants has been uniformly rejected by CMOS IC designers for thirty years because they have had no reason to employ it. Capacitive coupling has always been possible, but it is undesirable, because capacitors occupy a large amount of expensive IC area, and such coupling also requires provision of biasing circuitry. The Appellants have discovered a reason to use that which was previously rejected as undesirable. In particular, the Appellants discovered that creating a slow-edged clock waveform, and using the same slow-edged waveform to control

TCCSs, significantly reduces noise generation in a charge pump. Instead of being an impractically expensive alternative for coupling, capacitive coupling as claimed by the Appellants becomes the most efficient way to couple a slow-edged clock signal to the switches it controls. It has the advantage that it does not increase the dv/dt of the clock waveform, as would conventional coupling techniques. Thus, the Appellants have discovered that capacitively coupling the clock to the TCCSs can unexpectedly help reduce noise generation, if done properly.

Thus, the Appellants' discovery motivates the use of circuits that, while known, were undesirable and therefore avoided by all skilled designers. It renders desirable what was universally thought undesirable. Because the Appellants' discovery provides a new, different and unexpected motivation to do what could have been, but was not done in the relevant prior art, it is particularly important to consider the motivation when evaluating the nonobviousness of the Appellants' claims. The features claimed by the Appellants would have remained possible but not done, in the absence of some new motivation such as is provided by the Appellants' discovery.

The courts have long looked to the motivation to make a proposed modification to help distinguish the teaching of the prior art from a hindsight concatenation of existing features. *KSR* disapproved the rigid requirement for a motivation expressed by the TSM test developed by the Federal Circuit. In particular, the Supreme Court asserted that motivation could be provided by common sense or market forces, for example. But the Examiner has in general provided no motivation at all, whether common sense or otherwise, aside from a conclusory statement that it "would be obvious." Indeed, common sense and market motivations support the nonobviousness of the claimed feature combinations at the time of the invention: prior to the Appellants' discoveries in regard to noise, common sense and market forces both motivated the skilled designer to avoid the circuitry now preferred and claimed by the Appellants.

The Supreme Court also expressly noted the continued vitality of motivation for evaluating obviousness (underlining added for emphasis):

> When it first established the requirement of demonstrating a teaching, suggestion, or motivation to combine known elements in order to show that the combination is obvious, the Court of Customs and Patent Appeals captured a helpful insight. See *Application of Bergel*, 292 F. 2d 955, 956–957 (1961). As is clear from cases such as *Adams*, a patent composed of

> several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. *KSR Int'l. v. Teleflex Inc.*, 167 L. Ed. 2d 705, 722; 127 S. Ct. 1727, 1741 (2007).

To avoid improper hindsight and thus to fairly determine whether a claimed combination was obvious at the time of the invention, in the absence of the insight and motivation provided by the Appellants themselves, it is essential for the Examiner to identify some reasonable motivation for the changes to *thirty years of developed wisdom* in respect of charge pumps. The Examiner has not done so in almost any case (save in regard to three stage CSROs).

VII.A.4.d Attributing to References Features That Are Clearly Absent

The Examiner has persistently attributed disclosure to prior art references that are clearly devoid of such disclosure, sometimes urging that such disclosure is present precisely because the reference is so devoid of information that it does not preclude the possibility that such disclosure might have been used. The Examiner continues to make this error in current rejections, despite the Appellants having objected to this practice for literally years.

Alternative doctrines for considering apparently missing descriptive matter to be present in a cited reference include taking "official notice" and citing to "common knowledge." All such doctrines are construed very narrowly, lest the exception swallow the rule requiring substantial evidence to support conclusions. *In re Zurko*, 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Zurko III) (Fed. Cir. 2001) ("[D]eficiencies of the cited references cannot be remedied by the [reviewing entity's] general conclusions about what is "basic knowledge" or "common sense" to one of ordinary skill in the art."

This examination error is extremely serious because the Examiner attributes *important* subject matter to a reference that clearly has no such disclosure, and bases his justification for rejecting claims on such attributed, but nonexistent, disclosure.

It can be entirely proper to infer the presence of material not actually disclosed in a reference under a principle such as inherency. However, it is clearly improper to infer the presence of material which, far from being inherent (*i.e.*, necessarily implied in the context), is *contrary to the prior art as a whole and/or the reference in particular.*

For example, Tasdighi and Yamauchi disclose no details whatsoever of the electrical coupling between the controlling clock, and the switches (TCCSs) that they control. Both utilize a line, with or without an arrow, drawn between "clock" and "switch" blocks in a block diagram to indicate some sort of control is exerted by the clock over the switches. The line and/or arrow is NOT an electrical symbol, and does not, nor is intended to, convey any electrical information.

The Appellants completely agree that the absence of coupling information in these references implies that exerting such control is well known in the art of charge pumps. The Appellants vehemently disagree, however, that such absence of information indicates that the control is exerted by the features or techniques claimed by the Appellants. The absence of information may properly be filled in by reference to the prior art, but may NOT properly be filled in by reference to the claimed subject matter. There are many ways well known in the prior art to exert control by a clock over transfer switches, but most of them are *contrary to the requirements of the Appellants' claims*, or *would not work properly with the cited reference.*

One specific and egregious example of this erroneous examination practice is set forth in subsection *VII.B.9 Rejection as Obvious over Tasdighi in view of Yamauchi and Pfiffner*, incorporated here by reference.

As a somewhat shorter specific example, the Examiner rejects Claim 3 as obvious over Tasdighi in view of Yamauchi. Claim 3 requires in part (underlining added for emphasis): "[C]oupling circuitry configured to couple the particular charge pump clock output as a signal to each of the transfer capacitor coupling switches <u>without increasing a rate of voltage rise or fall of the signal</u>,". This is an important limitation that excludes most typical IC clock coupling circuitry, and is significant for reducing noise generation because it is best if not only the clock signal as initially generated, but also as it is propagated to the switches it controls, is limited as to the speed (or dv/dt) of the signal. As noted above, Tasdighi and Yamauchi are both devoid of detail of the electrical

coupling method by which the clock exerts control on the transfer switches. Nonetheless, the Examiner justifies his assertion that Tasdighi in combination with Yamauchi renders Claim 3 obvious in the following statement (Office Action mailed December 12, 2007, p. 30 last full sentence, emphasis added):

> Deeming the line coupling the clock output from charge pump clock generating circuit (24 of Tasdighi; Fig. 7 of Yamauchi) to the control nodes of transistors 26,27 as coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of [*sic*] voltage rise or fall, thus rendering claims 3-4 obvious.

The Appellants do not dispute that the line implies some sort of coupling circuitry. However, Appellants strongly object when the Examiner attributes specific characteristics to such unspecified coupling. In this case, the Examiner attributes a characteristic of not raising the dv/dt of the signal. Such a characteristic is not known to be consistent with the prior art, particularly in the circuits of Tasdighi and Yamauchi. The Appellants vigorously oppose the Examiner's penchant for thus attributing important material to a reference that is entirely devoid of the attributed material.

The Examiner has been improperly attributing absent material to references since the beginning of prosecution of the subject application. Such attribution is not merely inadvertent, because the Appellants have repeatedly objected to this practice by the Examiner (see, *e.g.*, Amendment mailed April 1, 2005, last paragraph p.25: "The lack of detail in Tasdighi does not permit a conclusion as to how the signal is coupled. In particular, the absence of detail cannot be fairly assumed to imply that Tasdighi provides a single-phase clock coupled passively to the switches;" and the Amendment After Final Rejection mailed October 11, 2005, subsection entitled *Attributing Specific Teaching Based on an Absence of Information in a Cited Reference*, six paragraphs beginning near the bottom of p. 15). Instead, it is a systematic error that the Examiner engages in repeatedly.

The Examiner has recognized the Appellants objections to attributing specific content where none exists. In his first Final Rejection, issued August 10, 2005, in the "Response to Arguments" section beginning on page 31, the Examiner identified the issue among a list of those raised by the Appellants, stating "5) the references of Tasdighi, Hara et al., and Ito do not show or disclose the claimed limitations, and therefore the claims are nonobvious." However, although he addressed the

preceding items 1-4, the Examiner failed to address this issue (5). Moreover, the Examiner complained (Office Action issued May 17, 2007 reopening prosecution, page 38 lines 9-10): "However, the applicants appear to want each reference to clearly show, and/or disclose, every single limitation being claimed, whether it is well known or not." The issue has also been a prominent subject of interviews. Thus, the Appellants have vigorously and repeatedly objected to rejections thus "supported" by a complete absence of disclosure in any reference cited in the rejection, but only for important subject matter that was not, contrary to the Examiner's contention, even likely to have been used in any actual implementation of the subject matter.

The detailed arguments in respect of specific grounds of rejection are set forth below.

VII.B. Rejections Under 35 USC § 103

The Examiner sets forth 115 rejections of 62 claims on 9 different grounds of obviousness, including 16 rejections of 7 independent claims on 7 different grounds of obviousness. Each is addressed in the following remarks.

VII.B.1 Rejections as Obvious over Imamiya in view of Pfiffner

On page 8 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 18-19, 49 and 70-71 as obvious over Imamiya in view of Pfiffner.

Each and every claim of the subject application requires a "charge pump" having an "output [voltage] supply." As may be seen from examination of the Appellants' application, a charge pump produces an output voltage supply. The output voltage supply is referenced in the body of each claim.

In each of a multiplicity of grounds of rejection that the Examiner sets forth over Imamiya in combination with one or more secondary references, the Examiner relies upon Figure 15A, or in this particular rejection Figure 15B, for a basic charge pump structure. The Appellants have pointed out [Appellants Response of September 17, 2007 to the Office Action reopening prosecution dated May 17, 2007, paragraph bridging pages 18-19] that Figures 15A and 15B of Imamiya do not illustrate a charge pump, and does not generate an "output voltage

supply" as required. Imamiya designates these circuits "potential converters" (*e.g.*, col. 4 lines 27-30), contradistinct from "charge pumps" that are also described (*e.g.*, col. 4 lines 49-52). The paragraph set forth below is from the Appellants' first response after appeal was originally initiated (Appellants' response mailed September 17, 2007, paragraph bridging pages 18-19, underlining added for emphasis):

> The Examiner points to Fig. 15B of Imamiya as showing a charge pump apparatus. It is respectfully submitted that Fig. 15B does not show a charge pump, but rather a "potential converter" (col. 4 lines 29-30), which is crucially different, and serves a very different purpose, from a charge pump. Potential converter details are illustrated in Figs. 7, 8, 9 and 15A-B, and used as item "5" in Figs. 4 and 14. Potential converters are disposed in series with a clock signal, rather like a buffer for upconverting a clock signal to a higher voltage (see item 5 of Fig. 4 with col. 5 lines 26-30, and items 5 of Fig. 14 with col. 10 line 35 - col. 11 line 29; see also col. 7 line 46 - col. 8 line 20). The output of potential converters is reset to zero every clock cycle; in the case of Fig. 15B, such resetting is performed by QN14.

The Examiner relies upon Figure 15A of Imamiya for the basic required features of "charge pump" and "output voltage supply," but Figures 15A and 15B are both "potential converters," which are not charge pumps and do not generate an output supply (see inset above). An "output [voltage] supply" is not reset to zero every clock cycle, as is the output of the potential converters described by Imamiya. As such, the Examiner's stated ground of rejection entirely fails to disclose the required elements of Claim 18.

The Appellants respectfully assert that the Examiner's interpretation of the term "output [voltage] supply" exceeds the bounds of "broadest reasonable interpretation." It should not be necessary to prove or explain the meaning of "output supply" to anyone of passing familiarity with electronic design, but if the Examiner finds the term ambiguous then he is urged to interpret the term in view of the disclosure of the Appellants' specification, in which it is invariably used to represent a largely constant reservoir of energy, and never to represent a widely varying control signal. Expert testimony on this point has not been, and cannot now be, offered, but if the panel finds this or any other factual matter in need of expert testimony for clarification, they are encouraged to identify such need to the Appellants. Any requested testimony will be provided as permitted by the BPAI, or upon remand.

The Examiner's insistence upon relying on Figures 15A or 15B of Imamiya (see inset paragraph (a) beginning p. 40 of Office Action mailed 12/12/2007) is particularly perplexing in view of the fact that the Appellants have pointed out to the Examiner that Imamiya discloses two types of charge pumps upon which the Examiner might have based an amended ground of rejection (Appellants Response of September 17, 2007 to the Office Action reopening prosecution dated May 17, 2007, paragraph bridging pages 19-20, underlining in original):

> Though the examiner's reliance on Figure 15B is unavailing because the figure does not illustrate a charge pump, the following remarks address two types of charge pumps disclosed in Imamiya, including one type in figure 5 and another type in figure 10, with respect to Claims 18-19 and 49. The charge pump of figure 5 uses passive transfer capacitor coupling switches (diode-connected FETs "QN"), has two clock phases φ and φ-inverse, and draws all output current from the clock outputs. Thus, this charge pump fails to disclose either the "control node" (of a TC discharge switch or output switching device), or the "single phase clock," both of which are required by each of Claims 18 and 49; and these omissions are not remedied by Pfiffner. The charge pump of figure 10 also fails to anticipate or render obvious (in combination with Pfiffner) these claims, though for different reasons. For example, the output voltage in Fig. 10 is switched via QN73, which is not controlled directly by or coupled directly to the clock. Due to this construction, the charge pump described by figure 10 of Imamiya fails to disclose several aspects of the requirements set forth in element (d) of the Appellants' Claim 18, including (underlining added for emphasis): "to provide a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, ... to control nodes of each of the output switching devices." Again, Pfiffner does not describe charge pumps and therefore cannot remedy these omissions by Imamiya, nor would it be obvious to draw features from the non-analogous art of Pfiffner. Consequently, Claims 18 and 49 are neither anticipated by, nor obvious over, the Imamiya and Pfiffner references, whether taken alone or together.

The paragraph inset above points out the most relevant charge pumps in Imamiya, and explains why Claim 18-19 and 49 are distinguished over the charge pumps of Imamiya in view of Pfiffner. However, it is not very constructive to argue against a rejection that the Examiner has declined to make.

The detailed grounds the Examiner sets forth to support his rejections over Imamiya are not comparable to, and do not disclose, the basic "charge pump" and "output supply" elements that are required by each and every claim of the subject application. Pfiffner does not remedy

those omissions. The Examiner's stated grounds of rejection thus wholly fail to render obvious the invention as claimed in any of the claims indicated above.

VII.B.1.a Rejection of Claim 18 over Imamiya and Pfiffner

Claim 18 requires (underlining added for emphasis):

> Charge pump apparatus for generating an output voltage supply within a monolithic integrated circuit, comprising:
>
> a) a transfer capacitor;
>
> b) one or more source switching devices disposed in series between the transfer capacitor and a voltage source to convey transfer current to the transfer capacitor from the voltage source when conducting;
>
> c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply to convey transfer current from the transfer capacitor to the output voltage supply when conducting; and
>
> d) a charge pump clock generating circuit configured to provide a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively, without conveying substantial transfer current, to control nodes of each of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices, wherein the charge periods alternate with, and do not overlap, the discharge periods.

As noted in the preliminary remarks in subsection *VII.B.1 Rejections as Obvious over Imamiya in view of Pfiffner*, incorporated here by reference, the grounds of rejection that the Examiner insists on asserting rely on portions of Imamiya that entirely fail to disclose the basic requirements of a charge pump having/producing an output voltage supply. Pfiffner also fails to disclose these elements. The ground of rejection argued by the Examiner thus entirely fails to render obvious Claim 18.

Claim 18 is distinguished over Imamiya in view of Pfiffner even when considering the actual charge pumps set forth in Imamiya, for at least the reasons set forth in the inset paragraph above (Appellants Response of September 17, 2007 to the Office Action reopening prosecution dated May 17, 2007, paragraph bridging pages 19-20, underlining in original). As such, Claim 18 is clearly not

rendered obvious by Imamiya in view of Pfiffner, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 18.

VII.B.1.b Rejection of Claim 49 over Imamiya in view of Pfiffner

Claim 49 requires (underlining added for emphasis):

> A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:
> a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and
> b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

As noted in the preliminary remarks in subsection *VII.B.1 Rejections as Obvious over Imamiya in view of Pfiffner*, the grounds of rejection that the Examiner insists on asserting rely on portions of Imamiya that entirely fail to disclose the basic requirements of a charge pump having/producing an output supply. Pfiffner also fails to disclose these elements. The ground of rejection argued by the Examiner thus entirely fails to render obvious Claim 49.

Moreover, even if the actual charge pump circuits that are set forth in Imamiya are considered, this combination of references does not render Claim 49 obvious. Figure 5 shows one charge pump in Imamiya, but the clock outputs are coupled directly to the TCs, contrary to the requirements of element (a). The other charge pump in Imamiya is illustrated in Figure 10.

In Figure 10 of Imamiya, only the last TC C71, in section (71-n), is coupled to the output (9) Vout via a TC discharging switch. The TC discharging switch is QN73, which is a diode-coupled FET that acts as a passive diode. The discharging switch of element (a), therefore, is not "under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch," as required by element (a).

Indeed, for direct connection of a single clock to TCCSs to work without causing simultaneous conduction, it is essential that at least one of the TCCSs be a passive device rather than

an active device; in such case, it does not meet the requirements of Claim 49. The prior art has generally dealt with this issue by using all active TCCSs, but using a different clock phase to drive at least one of the TCCSs.

Pfiffner teaches nothing in regard to switching TCCSs under control of a charge pump clock, and thus cannot remedy the important omissions of Imamiya in this regard. As such, the cited combination fails to disclose all of the important requirements set forth in Claim 49, thus failing to establish even *prima facie* obviousness of Claim 49. Claim 49 is accordingly nonobvious over Imamiya in view of Pfiffner, and the panel is therefore respectfully requested to reverse the Examiner's rejection of Claim 49 on this ground. The panel is also requested to particularly reverse the Examiner as to his stated rationale for rejection of Claim 49.

VII.B.1.c Rejection of Claims 19 and 70-71 over Imamiya in view of Pfiffner

Claim 19 is nonobvious over Imamiya in view of Pfiffner by virtue of depending from Claim 18 for the reasons set forth above with respect to Claim 18. Moreover, Claim 19 requires in part: "g) one or more second-output switching devices disposed in series between the second transfer capacitor and a second output voltage supply." None of the charge pumps of Imamiya (Figures 5 and 10) disclose a second output voltage supply. The circuit of Figure 15B, relied upon by the Examiner for this rejection, does not even disclose a first output voltage supply, let alone a second. Pfiffner also fails to disclose either first or second output voltage supplies. Thus, Claim 19 is further distinguished over Imamiya in view of Pfiffner for at least this reason. The panel is accordingly respectfully requested to reverse the Examiner as to this ground of rejection of Claim 19, irrespective of the patentability of Claim 18.

Claim 70 is nonobvious over Imamiya in view of Pfiffner by virtue of depending from Claim 18, for the reasons set forth above with respect to Claim 18. Moreover, Claim 70 requires in part: "each of the source switching devices and each of the output switching devices is a transfer capacitor ("TC") switching device, each such TC switching device is either an n-channel FET or a p-channel FET, and wherein threshold voltages of all n-channel TC switching devices are substantially similar, and threshold voltages of all p-channel TC switching devices are substantially similar. Imamiya

does not disclose these limitations; and Pfiffner does not disclose FETs at all, and hence cannot remedy the omissions of Imamiya in this regard.

The Examiner makes an egregious error in the grounds of rejection he sets forth for Claim 70. He asserts that because each switching device is either an N-channel or a P-channel FET, and "nothing in Imamiya shows or discloses different thresholds among the same conductivity FETs, claim 70 is rendered obvious." According to the Examiner's logic, an element is rendered obvious if a cited reference fails to disclose anything to the contrary. The Examiner's ground of rejection is, of course, contrary to the basic, essential requirement for establishing *prima facie* obviousness, that the cited combination of references must disclose each and every claimed limitation of the claim. The undersigned is simply astonished that after pointing out the impropriety of such reasoning for literally years, this Examiner continues to insist that a claim is rendered obvious when the cited references fail to disclose anything contrary to the cited limitation. The Examiner does not even suggest that either Imamiya or Pfiffner actually discloses these requirements of Claim 70, and indeed they do not.

At least barring the unusual condition that the clock driving the circuits of Imamiya goes far outside the rails (Vdd and ground), the circuits of Imamiya could not, in fact, function as intended if the threshold voltage was the same for both of the two N-channel FETs that are coupled in series with each transfer capacitor. But it is not the proper burden of the Appellants to prove that a prior art reference could not have employed a claimed feature. Instead, it is the burden of the Examiner to demonstrate that the cited prior art reference actually discloses each claimed limitation, a burden the Examiner does not even claim to have discharged.

In any event, because Imamiya and Pfiffner both fail to disclose, teach, or fairly suggest these limitations, Claim 70 is nonobvious over the combination of Imamiya and Pfiffner for this reason irrespective of the nonobviousness of Claim 18. As such, the panel is respectfully requested to and is base rejections on the wholly backward basis that wish to claim.

Claim 71 is nonobvious over Imamiya in view of Pfiffner by virtue of depending from Claim 49 for the reasons set forth above with respect to Claim 49. Claim 49 further requires features comparable to those recited in Claim 70. Imamiya and Pfiffner both fail to teach, disclose or fairly

suggest these limitations for substantially identical reasons as set forth above with respect to Claim 70. The Examiner explicitly states that his grounds for finding Claim 71 obvious is the same as he used for Claim 70. For these reasons, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 71.

VII.B.2 Rejections as Obvious over Imamiya in view of Ito

On page 10 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 1-4, 9-10, 12-14, 16-17, 28-33, 36-41, 43-45, 48, and 68-69 as obvious over Imamiya in view of Ito.

VII.B.2.a Examiner's Contentions in Support of Rejections over Imamiya in view of Ito

Remarks in subsection *VII.B.1 Rejections as Obvious over Imamiya in view of Pfiffner* are incorporated here by reference to demonstrate that the Examiner's contentions with respect to Imamiya, which rely on Figures 15A, are wholly misplaced. The subject matter described by the Examiner fails to disclose either a charge pump or an output supply (or output voltage supply) as required by each and every one of the claims rejected as obvious over Imamiya in view of Ito.

Ito fails to disclose these same features. Ito does not disclose a charge pump, but rather a voltage controlled oscillator (VCO); and a VCO outputs a signal, not a supply. Because both the contentions of the Examiner with respect to Imamiya, and the disclosure of Ito, fail to demonstrate a plurality of important specified limitations, the Examiner fails to establish *prima facie* obviousness for any of these claims. It does not make sense to argue details in respect of disclosure that fails to disclose even the basic requirements of the claims purported to be rejected thereby.

VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito

Though the Examiner has refused the Appellants invitation to base his rejection on actual charge pumps having output supplies in Imamiya (see inset paragraph (a) beginning p. 40 of Office Action mailed 12/12/2007), the Appellants address a general rejection over Imamiya in view of Ito in the remarks set forth below. The remarks set forth below are included for completeness, and of necessity cannot directly address the grounds of rejection that the Examiner asserts, which, as

demonstrated in the remarks set forth above, entirely fail to support *prima facie* obviousness of any pending claim.

A skilled designer would not modify charge pump designs of the prior art by substituting an oscillator from Ito that is different from all of the relevant teaching and examples set forth in the extensive prior art of charge pumps. One reason for this is that Ito is not analogous prior art, a conclusion supported by further remarks set forth below. A second, closely related reason is that there is no motivation for such a combination. A third reason is that not only is there no positive motivation for such a modification, there is express teaching in the prior art away from such combination. Even if a skilled designer sought oscillator design ideas from non-analogous art such as Ito, they would seek a particular range of clock output waveform, and would therefore specifically not follow the three stage current starved ring oscillator teaching of Ito. Each of these contentions are addressed in the following remarks.

Ito Is Nonanalogous Art And Would Not Be Followed for Charge Pumps. To establish *prima facie* obviousness of any claim over Imamiya in view of Ito, even when considering the actual IC charge pumps set forth in Imamiya, requires a conclusion that a skilled person would modify a charge pump in accordance with a voltage controlled oscillator reference. Remarks set forth above in subsection *VII.A.1.b Scope and Content of the Prior Art* are incorporated here by reference to support the contention that the very crowded field of charge pump prior art provides ample guidance, developed over the course of more than thirty years, which is known to be satisfactory for IC charge pump designs; and that a skilled person would therefore not, without special motivation, design contrary to such established practice. Ito is an example of prior art that is not analogous to charge pumps, and therefore would not be considered by a person of skill in the art to modify the teaching of the prior art of charge pumps.

Ito is an example of a general purpose voltage controlled oscillator that is not described as suitable for charge pumps. All manner of oscillators, having all manner of output waveforms, have been available for the entire multiple-decade period during which IC charge pumps have been designed by the hundreds. Well over a hundred charge pumps have been the subject of patents. Yet, as demonstrated by remarks set forth in subsection *V.A.2 Inventive Concept Differs Radically from*

Prior Art Teaching, incorporated here by reference, none of the IC charge pump prior art (insofar as can be seen from the extensive collection of charge pump references that is of record) from this entire period describes a charge pump clock having a slow output, much less an output that is substantially sine-like. Yet oscillators that produce various slow, even precisely sinusoidal outputs have been well known throughout the entire period of over three decades that IC charge pumps have been designed, prior to the Appellants' invention. If highly skilled and inventive IC charge pump designers have consistently avoided the use of a clearly available alternatives for decades, that fact speaks for itself to support a conclusion that IC charge pump designers have good reasons to avoid such available alternatives. The Appellants add that slow clocks are avoided by the prior IC charge pump prior art in part because high speed clocks, as compared to slow clocks, are much easier to process and control with tiny active circuit devices that are readily available in ICs. But even if the specific reasons submitted by the Appellants are not given weight, the principle of *res ipsa loquitur* supports a conclusion that charge pump designers would not use slow or sinusoidal clocks, on the evidence that they did not do so during the over thirty years of active development of IC charge pumps, despite such clocks being available for the entire thirty-plus years.

The conclusion that charge pump designers avoided using some clocks that were readily available, supported by the remarks above, supports a further conclusion that charge pump designers have limits on the scope of charge pump clocks that were believed suitable for charge pumps. Such scope of charge pump clocks is best indicated by examination of the large number of extant prior art charge pump references. Because so many charge pump clocks specified for use with charge pumps are available, and because charge pump designers eschew some clock outputs, it is reasonable to conclude that oscillators that are not specifically indicated to be suitable for charge pumps should be considered nonanalogous to charge pumps. Stated differently, there is no reason to assume that a random oscillator, demonstrably different from all oscillators in the prior art of charge pumps, is suitable for use with charge pumps.

The second contention is that there is no motivation to follow Ito to change a charge pump clock design to be different from previous charge pump clock designs.

No Motivation Exists For Modifying Charge Pump Prior Art According to Ito. A skilled designer might deviate from the wisdom of the large body of teaching directed expressly to charge pumps if a compelling reason to do so outweighed the risks inherent in going beyond the bounds of art known suitable for charge pumps. The Appellants, for example, were faced with a problem of noise that could render their product unusable in the market for which it was intended, which is strong motivation indeed. They were inspired by stark necessity to design contrary to the whole body of charge pump prior art. In their desperation, they envisioned that a slow, rounded charge pump clock output instead of the conventional square or nearly square clock output might help alleviate noise generation, and eventually developed the disclosure set forth in their application.

The Examiner presently sets forth no reason at all for a charge pump designer to deviate from the well developed teaching of the IC charge pump prior art. Instead, he essentially says simply that it is possible, and therefore would be done, a contention that is at odds with three decades worth of prior art. His current statement in respect to motivation is inset below (page 11, Office Action issued December 12, 2007 finally rejecting Appellants' claims, underlining added for emphasis):

> Although Fig. 15A does not clearly show a charge pump clock generating circuit, that provides charge pump clock output Ø, as a ring oscillator with an odd number of not more than three driver sections including circuitry to limit the rise and fall of each of the driver section's output, Imamiya does disclose the relationship between clock signals and an oscillator, such as a ring oscillator, for generating at least clock output Ø, used to control the plurality of transfer capacitor coupling switches of Imamiya, would be provided by some type of a charge pump clock generating circuit, such as a ring oscillator. Ito shows and discloses various examples of ring oscillators that provide a clock output. Therefore, it would have been obvious to one of ordinary skill in the art to utilize Ito's ring oscillator 70 (shown in Fig. 12) as the charge pump clock generating circuit/(ring) oscillator that provides charge pump clock output Ø to control Imamiya's plurality of transfer capacitor coupling switches.

The Examiner acknowledges that the clock Ø, for which no circuitry is disclosed in Imamiya, "would be provided by some type of a charge pump clock generating circuit." He then states that Ito shows clock generators circuits, and concludes that a skilled designer would therefore modify Imamiya in accordance with Ito.

A skilled automobile designer, faced with automobile teaching that does not detail the engine, would know that some sort of automobile engine was needed. Engine manufacturers

describe various engines, including jet engines and outboard motor engines. Therefore, the automobile designer would assume that the missing engine would obviously not be a jet engine. The skilled designer would, instead, assume that the engine was some sort of automobile engine. In the same way, a skilled charge pump designer would, as the Examiner acknowledges, recognize that the omitted source of the clock was "some type of charge pump clock generating circuit." Such skilled designer would not assume that any clock output must be a suitable clock output.

The Examiner does not presently even allege that there is any particular motivation for selecting a clock that is different from anything found in the extensive body of charge pump prior art, nor is there any. However, the reasonable conclusion of a skilled person is that there is reason behind a large body of IC charge pump teaching consistently avoiding very short ring oscillators. Such skilled person would therefore follow the charge pump teaching rather than randomly inserting circuitry that is demonstrably avoided in all prior art IC charge pumps.

Teaching Away From the Claim 1 Combination Exists, but No Teaching Toward It. The examples set forth in charge pump references of ring oscillators that conform to some of the features claimed for charge pump clocks of the rejected claims include a number of inverter stages in the ring oscillator, where the number ranges from a minimum of five (US patent 5,446,418, hereafter "Hara") to at least thirteen (US patent 5,182,529, hereafter "Chern"). But Chern describes a thirteen-stage ring oscillator as "typical," reciting (col. 1 lines 12-14, underlining added for emphasis): "A typical charge pump system 10 is shown in FIG. 1, including a ring oscillator 12 for providing a square wave oscillating signal to a charge pump 14." FIG. 10 is a thirteen-stage ring oscillator. Hara, to the contrary, indicates that five stages is a minimum, reciting (col. 5 lines 60-62, underlining added for emphasis): "Herein, the five stages of inverters are used to constituting [*sic*] the ring oscillator by way of illustration, but odd number stages more than five may be employed." No IC charge pumps of record, or known to the Appellants, disclose or otherwise suggest an example of a three stage current starved ring oscillator intended for use as a charge pump clock.

Acknowledging that three stage current starved ring oscillators are known for use in many circuits other than charge pumps, such as in Ito for a VCO, it is submitted that such oscillators would not be selected by a skilled designer for use in charge pumps. A charge pump designer might well

select a different oscillator than is commonly used in charge pump prior art, but he would select it to produce a desired clock waveform. No designer worthy of the name simply selects an oscillator at random because one is needed, and the Examiner's suggestion that it would be obvious to do so exceeds reason. At least two pieces of evidence support a conclusion that a skilled person would not follow Ito to employ a three inverter stage current starved ring oscillator. The first evidence is the fact that such a ring oscillator is not found in the extensive charge pump prior art developed over thirty years, despite the fact that ring oscillators are the most commonly used circuit for generating a charge pump clock. The second evidence is the fact that only one reference of record discloses even as few as five inverter stages, and that reference expressly suggests that five is a minimum.

A 3-Stage Current Starved Ring Oscillator Generates Undesirably Slow Output Waveform. The undesirability of a three stage current starved ring oscillator (CSRO) in a charge pump is apparent by it's notable absence from the prior art of charge pumps despite the fact that ring oscillators, even current starved ring oscillators, are commonly used. A technical reason for rejecting such ring oscillators is that fast-edged clock signals are *de rigueur* in charge pump design, and that a very short current starved ring oscillator tends to produce a slow-edged trapezoidal output waveform that is uncertain in timing and alignment, and is generally contrary to the fast-edged, squared clock signals that are demanded.

ICs, especially CMOS ICs, are able to process digital signals more efficiently and accurately than analog signals, because extremely tiny active circuits using almost zero power can accurately reproduce a simple digital signal with or without inverting and/or level shifting. Transmitting analog signals is difficult using active circuitry, generally requiring complex analog amplifier circuits. Capacitive coupling is possible but suffers from a lack of gain, a need for biasing circuitry, and occupation of large IC areas. Moreover, a plurality of different gate inputs accepting the same slow-edged waveform are likely to identify a transition between states at different voltages, which means that they will identify the transition at different times. To restate that point, transition voltage uncertainty translates to significant timing uncertainty when digital gates input a signal having a slow transition. Thus, a fast-edged clock signal is preferred, and a slow-edged clock signal may cause timing uncertainty, and digital signals are more readily processed.

Moreover, transfer capacitor (TC) charging switches (TCCSs) have limited gain, and cannot change from fully off to fully on until their control input voltage is changed by a significant amount. Therefore, a TCCS will spend less time fully "on" or fully "off" when driven by a slower waveform that spends proportionally more time transitioning between voltage extremes. To avoid damaging "shoot-through" or "simultaneous conduction," "charging" TCCSs must be fully off before "discharging" TCCSs may be permitted to be on at all, and conversely. For both of these reasons, slow control waveforms reduce the proportion of time during which the TC can conduct to either charge or discharge. Due to the factors set forth in this and the preceding paragraph, slow clock waveforms are undesirable for a conventional charge pump. These factors lead to a strong preference for a square or nearly square waveform for the charge pump clock.

The nature of current starved ring oscillators is such that as the number of stages is *reduced*, the proportion of time the waveform is in transition *increases*. This has been pointed out by the Appellants on a number of occasions, and the Examiner has not disagreed, going so far as to use the logic as a basis to conclude that the waveform from a three stage CSRO in Ito will be "substantially sine-like." (Appellants agree that a 3-stage CSRO will produce a relatively slow clock waveform, but they do not agree that a 3-stage CSRO will necessarily produce a substantially sine-like waveform, as specifically required in some claims.)

The half-period of a CSRO output equals the sum of stage delays. Thus if each stage delay is 1 μS, the half-period of an n stage ring oscillator is n * 1μS, for a total period of $2n$ μS. The proportion of a stage delay due to a threshold transition time (time to move from one voltage extreme to the threshold voltage) can be varied depending, for example, on the drive current limits and the amount of capacitance loading the output of each inverter. If the threshold is set to the middle of the voltage extremes, it may also be seen that total transition from one voltage extreme to the other will be twice the threshold transition time. Assuming for illustration that the threshold transition time accounts for 70% of the total stage delay, it may be seen that total transition from one output voltage extreme to the other takes 1.4 μS, so that both transitions occupy 2.8 μS. The output of a five-stage CSRO under such circumstances would spend 2.8 μS in transitions out of a total period of 6 μS, thus being in transition 47% of the time. The output of a corresponding three stage CSRO would spend 2.8 μS in transitions out of a total period of only 4 μS, thus being in transition

70% of the time. As may be seen, the proportion of time spent in transition for a CSRO output changes dramatically as the number of stages becomes small. Stated differently, the output rapidly becomes less square as the number of stages decreases to a small number.

The remarks set forth above demonstrate, first, that a slow waveform is undesirable for charge pumps, and second, that a CSRO having a small number of stages will produce a slow waveform. As such, it is clear that CSROs having a very small number of stages will tend to produce a waveform that is undesirable for conventional charge pump designs. The Appellants will provide expert explanation of this issue upon request from the panel.

A Skilled Designer Will Select An Oscillator Based On the Desired Waveform. No electronic circuit designer, faced with a need to provide a clock, would simply pick one at random from those within or without the field of charge pumps. Instead, such designer would select the oscillator that provided a suitable waveform. As such, given that the conventional wisdom of charge pumps holds that slow-edged clocks are generally undesirable, such designer would not select a three stage CSRO as the oscillator for a charge pump. The Examiner's bald assertion that it would be "obvious" to use a three stage CSRO just because it exists in the field of electronics, though outside the field of charge pumps, reflects a complete misunderstanding of the job of a circuit designer.

The remarks set forth above demonstrate a variety of points. First, Ito is nonanalogous to charge pumps and would not be followed to modify a charge pump. Second, no motivation exists for modifying charge pump prior to conform to Ito rather than to the wisdom of IC charge pumps developed over a period of more than thirty years. Third, the prior art of charge pumps does not have any teaching toward a charge pump using a current starved ring oscillator of only three stages; and, to the contrary, it has express teaching away from such a feature. The Appellants submit that the technical reason for the undesirability of 3-stage CSROs is that they tend to generate a slow-edge output waveform that is demonstrated to be undesirable for charge pumps. In any event, a skilled designer will not combine prior art circuits randomly, but will select an oscillator that will produce a desired waveform. Because waveforms such as result from a 3-stage CSRO are undesirable for charge pumps, 3-stage CSROs are consequently undesirable. For all the foregoing reasons, a skilled designer would not follow Ito to select an oscillator for a charge pump; or, if a skilled designer

wished to select an oscillator from Ito, the oscillator selected would not be a three stage CSRO, as the output is inimical to conventional charge pump design wisdom.

The decision by the Appellants to contravene the well established conventional wisdom of charge pump design is explained in detail in the subject application. The new features enable the Appellants to reduce the noise generated by charge pumps, which can be critical in some applications. However, because noise is an unintentional creation, reducing noise is very unpredictable. Nobody would have guessed the advantages that the Appellants have discovered for such features as a 3-stage CSRO clock, capacitive coupling of the clock to the TCCSs, or a substantially sine-like clock output. These features have always been possible to implement, but have always been considered undesirable, and, consequently, have been universally avoided.

In the next subsection, the present facts, together with the conclusions developed and supported above, are compared to the facts and conclusions developed in the widely cited case *W.L.Gore*.

VII.B.2.c W.L.Gore Compared to Rejections Over Imamiya / Ito and Forbes / Ito

The remarks set forth or incorporated by reference in the preceding subsection, *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*, are incorporated here by reference as support for a contention that Ito is nonanalogous art that would not be followed by a skilled person to modify a charge pump contrary to the extensive and well established conventional practice of charge pumps. The incorporated remarks are also pertinent to a comparison, set forth below, of the present facts to the facts and conclusions at bar in the case of *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert denied*, 469 U.S. 851 (1984) ("*W.L.Gore*"). *W.L.Gore* has been cited over 600 times in judicial decisions, including over 100 times in Federal Circuit decisions, without eliciting a significantly negative comment, with the exception of cases that were overruled on appeal, and is thus very strong law. A comparison of the present facts to those at bar in *W.L.Gore*, as set forth below, is a different route that leads to the same conclusion of nonobviousness as do the remarks incorporated above.

The following is an introductory summary of contentions; the relevant facts and citations are set forth subsequently to support each contention. The law as set forth in the Federal Circuit opinion in the case of *W.L.Gore* requires the fact-finder to weigh the teaching of all of the prior art, including art that teaches away from the claimed limitation. "In its consideration of the prior art, however, the district court erred in ...; and in considering the references in less than their entireties, i.e., in disregarding disclosures in the references that diverge from and teach away from the invention at hand." *W.L.Gore* at 1550, citing *In re Kuderna*, 57 C.C.P.A. 1078, 426 F.2d 385, 165 USPQ 575 (CCPA 1970), emphasis added.

Because the prior art of charge pumps provides no teaching of the claimed feature at issue (a current starved ring oscillator employing not more than three inverter stages), but includes teaching away from that claimed feature, *W.L.Gore* requires a conclusion that a claim characterized by such claimed feature is not rendered obvious merely because the claimed features may be separately found in prior art (Ito) that is not directed to charge pumps. The following exposition thoroughly supports this conclusion for two combinations of references that the Examiner asserts render Claim 1 obvious: Imamiya with Ito, and Forbes with Ito.

Reference Combinations That Fail to Render Obvious Claims in W.L.Gore, Compared to Reference Combinations Asserted as Rendering Obvious Rejected Claims. The combination of Imamiya in view of Ito (or Forbes in view of Ito), considered as it must be in view of other prior art (*W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), "*W.L.Gore*"), fails to render obvious the Appellants claimed combination of features that include a limitation to a charge pump clock comprising a current starved ring oscillator employing not more than three inverter stages, for the same reasons that the combinations of Sumitomo/Markwood and Smith/Markwood failed to render obvious claims (particularly claim 3) at issue in *W.L.Gore*. The present facts are set forth with respect to the rejection specifically of Claim 1 (over Imamiya in view of Ito, or over Forbes in view of Ito), as representative of any claim that is distinguished at least by the three stage current starved ring oscillator. These present facts are closely analogous to those of *W.L.Gore*, and, as such, the court's reasoning there is readily applied to the present facts.

Claims 3 and 19 of Gore's '566 patent were particularly at issue in *W.L.Gore*. The holding by the lower court that claim 3 was obvious over (a) Japanese patent 13560/67 (Sumitomo) with U.S. patent 3,214,503 (Markwood); and (b) U.S. patent 2,776,465 (Smith) with Markwood (*W.L.Gore* at 1546), is most analogous to the present rejection of Claim 1 over (a) Imamiya with Ito, and (b) Forbes with Ito.

Primary references cover basic subject matter of claim but are silent about a magnitude limitation. In *W.L.Gore*, the primary references Sumitomo and Smith both expressly disclosed processing of unsintered PTFE, the basic subject of claim 3 (*W.L.Gore* at 1551). Similarly here, both Imamiya and Forbes expressly disclose teaching in respect of charge pumps (though not in the portions of Imamiya pointed to by the Examiner), the basic subject of Appellants' Claim 1. In *W.L.Gore*, both primary references were silent in respect of the magnitude limitation on rate of stretch ("In respect of claim 3, neither reference mentions rate of stretch or suggests its importance." *W.L.Gore* at 1552). Similarly here, Imamiya and Forbes are completely silent in respect of charge pump clock oscillator details, and in particular in respect of the magnitude of a number of inverters in a ring oscillator.

Common secondary reference relied upon for a parameter range limit. In view of the silence of the primary reference in respect of the magnitude limit, a colorable basis to support a finding of obviousness requires a reference suggesting the claimed magnitude limitation. In *W.L.Gore*, the common secondary reference, Markwood, was relied upon for a range (magnitude) limit on a process parameter (a magnitude on rate of stretching, encompassing the claimed 100% per second, *W.L.Gore* at 1551); here, the common secondary reference, Ito, is relied upon for a magnitude limit on a circuit parameter (not more than three inverter stages in a ring oscillator for a charge pump clock).

Secondary reference describes a context differing from the claimed subject matter. In *W.L.Gore*, the stretching rate taught by Markwood was in a process that was not the same (thermoplastics) as the process claimed in claim 3 (unsintered PTFE) (*W.L.Gore* at 1551). Similarly here, the ring oscillator in Ito is for a different use (VCO) than the use of the ring oscillator claimed in Claim 1 (charge pump clock).

Prior art of the claimed subject matter as a whole found devoid of suggestion for the claimed combination, and in fact contained some teaching away. In *W.L.Gore*, the prior art of unsintered PTFE processing was found to provide no suggestion of an advantage for rapid stretching as claimed (*W.L.Gore* at 1551). Similarly here, the prior art of charge pumps has no suggestion of an advantage for a very short ring oscillator. In *W.L.Gore*, the prior as a whole was found to lead away from the claimed combination ("U.S. patent 2,983,961 to Titterton, Volume 13 of the Encyclopedia of Polymer Science and Technology (1970), the Sumitomo patent, and witnesses for both parties, establish that teachings related to conventional thermoplastic polymers are inapplicable to PTFE." *W.L.Gore* at 1550). Similarly here, the prior art as a whole teaches away from the claimed combination by virtue of the abundance of prior art with examples that are all contrary to the claimed limitation, plus express teaching by Hara that any odd number of inverter stages is suitable *except* the number of stages preferred and required by the Appellants (not more than three). Thus, as in *W.L.Gore*, the prior art of IC charge pumps, taken as a whole, teaches away from the claimed magnitude limitation.

Moreover, the available evidence reflecting thirty years of IC charge pumps is completely devoid of any very slow-edged clock, indicating a strong avoidance of a slow-edged clock. A very short ring oscillator will tend to create a clock for which the transition time is a large proportion of the total time of the clock period. The undesirability of slow-edged clocks is described in subsection *VII.A.2.a Integrated Circuit Charge Pump Clock Waveforms*, incorporated here by reference. It is reasonable to infer, from the technical fact of increasing proportions of transition time with shorter ring oscillators, and the evident avoidance of slow-edged clocks, that short (three stage) current starved ring oscillators are undesirable precisely because slow-edged clocks are undesirable. This reasonable inference further buttresses a conclusion that the prior art as a whole teaches away from the claimed current starved ring oscillator of not more than three stages.

W.L.Gore stands for the proposition that when there is no example or suggestion of a particular combination of features, the teaching of the prior art as a whole must be considered in deciding whether the combination would be obvious.

> Nowhere, in any of the references, is it taught or suggested that highly crystalline, unsintered PTFE could be stretched at a rate of about 100% per second as required by asserted claim 3.

> Nor is it anywhere suggested that by rapid stretching a PTFE article be stretched to more than five times its original length as required by asserted claim 19. On the contrary, the art as a whole teaches the other way.
> *W.L.Gore* at 1551, rationale for a finding of nonobviousness

It is respectfully submitted that the Examiner would not: (a) deny that Hara teaches away from the claimed combination; (b) deny that Ito is not directed to charge pumps; (c) deny that both Imamiya and Forbes are silent in regard to the requirement of a current starved ring oscillator having not more than three stages to produce the charge pump clock; (d) deny that he has been unable to locate a single example of an oscillator intended for use in a charge pump that employs only three stages in a current starved ring oscillator; or (e) deny that IC charge pump art prior to the Appellants' invention spans thirty years and hundreds of patents.

Thus, the facts before the court in *W.L.Gore* are very closely analogous to the present facts pertinent to the rejection of Claim 1 over Imamiya in view of Ito and over Forbes in view of Ito. The facts set forth above are believed to be generally uncontested, as indicated. Accordingly, under the law and reasoning of the venerable case *W.L.Gore*, Claim 1 should properly be held nonobvious over both Imamiya in view of Ito, and over Forbes in view of Ito.

The proposed motivation for the claimed combination has been ignored for thirty years in a crowded field, and thus underscores the undesirability of the claimed combination. The Examiner proposes a motivation for using only three inverter stages in a ring oscillator for a charge pump: that it would require less parts, and consequently occupy less space than a ring oscillator using more inverter stages. The Appellants acknowledge this basic advantage. However, the same advantage has been apparent to all skilled designers during the entire period of over three decades during which IC charge pump prior art has been actively designed and developed, yet has not resulted in a single example of such a short ring oscillator being used to generate a charge pump clock. If some change had occurred to introduce this motivation more recently, it could be said that only that reduced portion of the entire prior art, subsequent to such change, was developed in the actual knowledge of such a benefit. However, that is not the case. Every single IC charge pump designer, since the earliest IC charge pumps in the early 1970s, has been aware of this basic advantage, yet has nonetheless chosen to avoid such short ring oscillators.

The only reasonable inference that can be drawn from this fact, given the volume of charge pump prior art actively developed for over thirty years, is that a three stage current starved ring oscillator provides a very undesirable result. The Appellants respectfully submit that the most important reason for the persistent avoidance of a very short current starved ring oscillator is that such an oscillator produces an undesirable waveform. In particular, it produces a clock waveform with edges too slow to be suitable for the active coupling that is greatly preferred because of the ease with which it can be accomplished in ICs, especially CMOS ICs.

Irrespective of the reason offered above by the Appellants, *res ipsa loquitur* applies, such that this proposed motivation, in view of being ignored for thirty years of active development, becomes further evidence of the undesirability of using a very short ring oscillator for a charge pump. It simply cannot be obvious to do what has been actively resisted by highly skilled designers, faced with the same apparent motivations, for over thirty years.

However, while the motivations to use a short ring oscillator have not changed for other skilled persons during thirty years of charge pump development, they have changed for the Appellants. What changed for the Appellants, at the time of the invention, was their unpredictable discovery of a causal relationship between charge pump clock output waveform and noise generation by a charge pump. The Examiner does not suggest that anybody else discovered this relationship. In light of that discovery, and only in light of that discovery, a variety of previously rejected designs suddenly were seen by the Appellants to be desirable. Skilled persons unaware of the advantage taught by the Appellants still have no reason to employ the claimed features in a charge pump.

VII.B.2.d Rejection of Claims 1 and 43, plus 2-4, 10, 44-45, 48 and 68-69 over Imamiya + Ito

Claim 1 recites (underlining added for emphasis):

> Charge pump apparatus for generating an output voltage supply within a circuit, comprising:
> a) a transfer capacitor;
> b) a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output; and
> c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of not more than three inverting driver sections cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first

driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches, and wherein each driver section includes

i) circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output, and

ii) circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output;

d) wherein the plurality of transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times.

Claim 43 recites (underlining added for emphasis):

A method of generating an output supply by alternately transferring charge from a source voltage to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging switch circuit under control of a first charge pump clock output;

b) limiting source current provided to each inverting driver output node of a current starved ring oscillator having not more than three inverting driver stages within a first charge pump clock generator circuit by means of a corresponding source current-limiting circuit; and

c) limiting sink current drawn from each of the inverting driver output nodes by by means of a corresponding sink current-limiting circuit;

wherein the inverting driver output node of one of the not more than three inverting driver stages of the first charge pump clock generator circuit is the first charge pump clock output.

As may be seen, both Claim 1 and Claim 43 include limitations to a charge pump, and to the charge pump having an output [voltage, in Claim 1] supply. As such, the Examiner's contentions with respect to Imamiya fail to support *prima facie* obviousness of either of these claims for the simple reason that both references (Imamiya and Ito) fail to disclose important limitations of both claims.

Moreover, as may be seen in (c), (c)(i) and (c)(ii) of Claim 1, and in (b) and (c) of Claim 43, both claims include limitations such that the remarks set forth above require a conclusion that Claims 1 and 43 are nonobvious over Imamiya in view of Ito. Imamiya does not disclose any of the charge pump clock limitations; and while Ito discloses those limitations, it is in another context, for a general purpose VCO, and certainly not for charge pumps. The Examiner provides no motivation or reason for a skilled designer to ignore the extensive IC charge pump prior art, developed over more

than thirty years of making IC charge pumps, to follow VCO art. Moreover, the Examiner ignores teaching in the prior art (Hara) that is contrary to the asserted combination. The Appellants have repeatedly pointed out to the Examiner that Hara teaches that a charge pump clock circuit should have five or more inverter stages (see, *e.g.*, page 23 lines 2-3 of Amended Appeal Brief mailed January 5, 2007; and page 25 lines 5-7 of Amendment After Reopening Prosecution mailed September 17, 2007).

For all these reasons, the Examiner's rejection of Claims 1 and 43 is highly analogous to the rejections in *W.L.Gore* of claims over Sumitomo in view of Markwood, with the exception that Imamiya is less close to Appellants' Claim 1 than Sumitomo is to the claims at issue in *W.L.Gore*. As such, the reasoning and law of *W.L.Gore* compel a conclusion that Claims 1 and 43 are nonobvious over Imamiya in view of Ito, even considering the actual charge pumps of Imamiya.

The other arguments set forth above in subsections *VII.B.2.a Examiner's Contentions in Support of Rejections over Imamiya in view of Ito*, and *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*, incorporated here by reference, also clearly apply to support a conclusion that Claims 1 and 43 are nonobvious over Imamiya in view of Ito. For all of the reasons set forth above or incorporated by reference, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 1 and 43.

For purposes of this ground of rejection, Claims 2-4, 10 and 68 may stand or fall with independent Claim 1, and Claims 44-45, 48 and 69 may stand or fall with independent Claim 43.

VII.B.2.e Rejection of Claims 12 and 28, 13-14, 16, 29-33, 36, 38 and 40-41 over Imamiya + Ito

Independent Claims 12 and 28 are directed to charge pumps having an output supply. As such, the Examiner's contentions as to why Imamiya may be relied upon for disclosure of charge pump circuitry are incorrect for reasons set forth previously. However, Imamiya does disclose charge pumps, and the remarks set forth below ignore the Examiner's incorrect contentions with respect to the disclosure of Imamiya, and address instead the actual charge pumps described in Imamiya.

Ito would not be combined with Imamiya for all of the reasons set forth above in subsection *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*, which are incorporated here by reference.

Most importantly, however, neither Imamiya nor Ito disclose or suggest requirements characterizing Claims 12 and 28, which respectively recite, in part: "a voltage waveform of the charge pump clock output to be substantially sine-like," and "a voltage of the first charge pump clock output is substantially sine-like." As such, this combination of references fails to disclose extremely important elements of Claims 12 and 28, and accordingly fails to support *prima facie* obviousness of either claim.

The Examiner relies upon Ito for the "substantially sine-like clock output" required by both Claims 12 and 28. To justify his reliance on Ito as to Claim 12, the Examiner states (Office Action mailed December 12, 2007, page 13 lines 7-9, underlining added for emphasis): "The periodic switching of 61,53a and 53b,64 will effectively provide a waveform that is substantially sine-like (e.g. not a true square wave) due to the current limiting of 61 and 64, and capacitance 53c."

The Examiner does not even allege that Ito discloses an output that is "substantially sine-like," except by virtue of his oft-repeated assertion that any waveform that "is not a true square wave" is, for that reason alone, "substantially sine-like." Ito does not even expressly suggest that the output "is not a true square wave," though the Appellants acknowledge that there is no such actual waveform as a "true square waveform," because all waveforms have finite rise and fall times, and also acknowledge that the circuitry of Ito is likely to produce a significantly imprecise square wave.

Meaning of "Substantially Sine-Like" This subject is addressed in the remarks set forth in subsection *VII.C.1 Meaning of the phrase "Substantially Sine-like"*, which are incorporated here by reference. Those remarks support a conclusion that a skilled person would readily understand that a waveform that is "substantially sine-like" has a cycle comprised of four quarter cycles that are significantly symmetrical with each other, comprised of two half cycles that are significantly symmetrical with each other, has no significant straight line segments, and has no significant sharp angles.

No waveform in the extensive prior art of record suggests a waveform as the output of a clock for a charge pump that has a waveform that can remotely be called "substantially sine-like," especially when one considers what necessarily follows from the plain meaning of the term that clearly means "substantially like a sine wave." Even less does either Imamiya or Ito disclose such waveforms. The Examiner merely conjectures, again, that the three stage current starved oscillator shown in Ito would produce a "substantially sine-like" waveform. However, that conjecture is not only an improper basis for rejection, but is moreover simply incorrect, as the Appellants know from personal experience building such devices.

In view of the foregoing, it is clear that the Examiner does not point to any disclosure in Ito that can reasonably be said to suggest a "substantially sine-like" output. As such, Claims 12 and 28 are clearly not rendered obvious by the combination of Imamiya and Ito.

The W.L.Gore Decision Again. If the teaching of Ito were deemed to suggest a "substantially sine-like" output waveform, then many other references that are much more apposite would also suggest a "substantially sine-like" output. As such, the manifold improprieties of a rejection based on Imamiya in view of Ito are somewhat moot. However, the Appellants wish to note that even if Ito were *arguendo* deemed to disclose a "substantially sine-like" output, the cited combination would still not render obvious either of Claims 12 or 28 due to the legal requirements defined by *W.L.Gore*, as well as due to the many other reasons already set forth above by reference to subsection *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito.*

The prior art of charge pumps fails to suggest a charge pump clock waveform that is substantially sine-like. Even were Ito deemed *arguendo* to disclose such a waveform, Ito, even more than the Markwood reference in *W.L.Gore*, is not applicable to the basic process claimed. The Examiner has not described any motivation whatsoever for diverging from the conventional teaching of the field. In the absence of some motivation, a skilled person would not ignore the teaching of his art. The opinion of *W.L.Gore* recites in part (underlining added for emphasis):

> Having learned the details of Dr. Gore's invention, the district court found it within the skill of the art to stretch other material rapidly (Markwood); to stretch PTFE to increase porosity (Sumitomo); and to stretch at high temperatures (Smith). The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a

> mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic. On the contrary, the references and the uncontested testimony, as above indicated, established that PTFE is *sui generis*. It is not surprising, therefore, that, unlike the situation in *Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983),* there was no testimony and no finding that one skilled in the art would transfer conventional thermoplastic processes to those for unsintered PTFE, or would have been able to predict what would happen if they did.
> To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.
> *W.L.Gore* at 1552

The remarks set forth or incorporated by reference in subsection *VII.B.10 Supporting Remarks: Analysis of Clock Waveforms in Prior Art of Record* are incorporated here by reference for their support of a contention that no IC charge pump prior art, so far as can be deduced from the numerous references of record, discloses or suggests that a substantially sine-like charge pump clock output is suitable for controlling switches in an IC charge pump.

Thus, to modify a charge pump to employ a substantially sine-like clock waveform, as the Examiner asserts is obvious, the skilled designer would have to "disregard the teachings" of the prior art. *W.L.Gore* stands for the proposition that a skilled person would not do that without good reason, which the Examiner has not shown, especially in view of contrary teaching, which Hara provides.

Moreover, even if Ito taught a sine-like waveform output (Ito does not, but the Appellants do not dispute that such waveforms are taught for many other purposes in the electronic arts), Ito is not taught as applicable to charge pumps, just as Markwood is not taught as applicable to unsintered PTFE. Like in *W.L.Gore*, one skilled in the art would not transfer conventional oscillator waveforms to charge pump clocks, and would not know what would happen if it was done.

Except that the situation with substantially sine-like waveforms is that, insofar as they were used with otherwise conventional charge pump designs, they most like would not be satisfactory. Every prior art IC charge pump (as represented by the art of record) is designed for use with a clock output that is square, or nearly square. Circuits to be controlled by such waveforms expect relatively

sharp edges, and may not provide proper timing or consistency in response to a sine-like waveform. Moreover, it is practically inescapable that the conduction time, during which the fly capacitor is charged or discharged, will be significantly reduced as a fraction of the available time, increasing currents and losses and reducing efficiency. These are expected penalties. The Appellants have, in part, significantly redesigned the charge pump drive circuits in order to mitigate such penalties; but a need for extensive redesign does not help to render a modification obvious. The Appellants have also absorbed some penalties having to do with less than full conduction over significant fractions of the charge and discharge periods.

Both a need for substantial redesign, and tolerance of disadvantages, are penalties that the Appellants have absorbed to gain the advantage of noise reduction that is essential to their purposes. However, there is not the least hint in the prior art that such benefits would accrue from using a sine-like clock output; the advantages are taught only in the Appellants' application. In the absence of such expected benefits, a skilled person would certainly not be motivated to absorb such penalties. Modification to employ a substantially sine-like clock output waveform is therefore far from obvious.

The Examiner's proposed modification (assuming *arguendo* and contrary to fact that Ito teaches a substantially sine-like clock output) requires a designer to ignore known drawbacks to the claimed combination, in the face of a complete absence of any known advantage. Under those circumstances, the *W.L.Gore* decision supports a conclusion that the proposed modification to use a substantially sine-like clock is obvious to the Examiner only by dint of using the Appellants' claims as a frame, and thus had succumbed to the siren call of hindsight to assert as obvious that which, on a fair view, is clearly not taught or suggested by the prior art. As such, no art similarly not directed to charge pump clock outputs, which disclosed a "substantially sine-like" output, could properly be combined with Imamiya (or other charge pump art), to render obvious either Claim 12 or Claim 28.

In summary: Ito and Imamiya both entirely fail to suggest a "substantially sine-like" clock output, as required by Claims 12 and 28. Even if Ito did have such disclosure, Ito would not be combined with Imamiya for the various reasons set forth in subsection *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*. In particular, if Ito disclosed a

substantially sine-like output, the facts would then, at best, be quite comparable to those obtaining in *W.L.Gore*, and Imamiya combined with Ito would be held not to render Claims 12 and 28 obvious due to the lack of teaching of any advantages for the combination, combined with lack of teaching in the prior art of the combination, and with clear disadvantages indicated for such a combination. For all of these reasons, it is respectfully submitted that Claims 12 and 28 are nonobvious over Imamiya in view of Ito, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claims 12 and 28.

For purposes of this ground of rejection only, Claims 13-14 and 16 may stand or fall with independent Claim 12, and Claims 29-33, 36, 38 and 40-41 may stand or fall with independent Claim 28.

VII.B.2.f Rejection of Claims 9, 17, 37 and 39 over Imamiya in view of Ito

Claim 9 is nonobvious over Imamiya in view of Ito by virtue of depending from Claim 1, for all the reasons that Claim 1 is nonobvious over this combination of references set forth, or incorporated by reference, in subsection *VII.B.2.c Rejection of Claims 1 and 43, plus 2-4, 44, 48 and 68-69 over Imamiya in view of Ito*, above. Claim 17, by virtue of depending on independent Claim 12, and Claim 37, by virtue of depending on independent Claim 28, are nonobvious over this combination of references for all the reasons set forth with respect to independent Claims 12 and 28 in subsection *VII.B.2.d Rejection of Claims 12 and 28, plus 14, 16, 29-33, 36 and 38-41 over Imamiya/Ito*, above.

Claim 9 further requires in part: "wherein the active current limit circuitry of (c)(i) and (c)(ii) is further configured to limit source and sink currents, conducted by each driver section within the charge pump clock generating circuit, to substantially identical magnitudes." Claims 17 and 37 set forth substantially similar requirements. Imamiya discloses no details in respect of charge pump clock generation, and Ito does not disclose, teach or fairly suggest the requirements set forth in any of Claims 9, 17 or 37.

In regard to this ground of rejection of Claim 9, the Examiner points (Office Action issued December 12, 2007, page 12 beginning line 11) to "the current mirror configurations shown in Ito's

Fig. 12." He points out correctly (underlining added for emphasis) "the sink currents through transistors 62-64 will correspond to the currents flowing within transistors 56-57," and continues "the source currents through transistors 59-61 will correspond to the current flowing within transistor 58. With transistors 58 and 57 coupled in series between Vdd and Vss, their currents will be the same." The Examiner's assertions are literally correct, but they do not lead to his conclusion that Ito suggests the source and sink currents will have substantially identical magnitudes. Ito expressly teaches, to the contrary (Ito, col. 2 lines 16-28, specifically lines 25-28, underlining added for emphasis): "[I]nto the N-channel transistors 62, 63 and 64 for current controlling, there flow currents proportional to respective size ratios of the transistors 62, 63 and 64 to the transistor 57 (or the transistor 56)," and similarly with respect to the source current limiting transistors. Thus, Ito not only fails to suggest that the currents should have identical magnitude, but expressly points out that the magnitudes may be different in each case, depending on the relative sizes of the transistors. Ito does not suggest any particular relative sizes for the transistors in question, or otherwise suggest one or more particular current ratios.

The Examiner supports his rejection of Claim 17 only by referencing his arguments with respect to Claim 9, and supports his rejection of Claim 37 with reasons that are a subset of those he sets forth with respect to Claim 9. As such, and because Claims 17 and 37 set forth similar requirements as Claim 9, Claims 17 and 37 are additionally nonobvious over their respective independent claims for the reasons set forth in the preceding paragraph. Claim 39 is nonobvious for the same reasons as Claim 37 from which it properly depends.

Because Ito (as well as Imamiya) fails to suggest the requirements set forth in any of Claims 9, 17 or 37, but instead teaches to the contrary, these claims are each additionally nonobvious over their respective independent claims for the reasons set forth above. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of each of Claims 9, 17, 37 and 39.

VII.B.3 Rejections as Obvious over Imamiya in view of Ito and Yamashiro

On page 16 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 5-8, 15, 34-35, 46-47, 49 and 54-59 as obvious over Imamiya in view of Ito, and further in view of Yamashiro. The combination of Imamiya and Ito has been addressed above.

Yamashiro does not disclose a charge pump, or even an oscillator, but a linear amplifier fabricated from discrete components. It has very little in common with the subject of the invention, aside from using the most basic library of electronic components, including resistors, capacitors, and transistors. The transistors are FETs, but not MOSFETs on an IC, but discrete MISFETs. There is no common problem, no reason whatsoever for a skilled person to turn to such art to modify a charge pump.

Remarks set forth above in subsection *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito* are incorporated here by reference because, applied *mutatis mutandis*, the rationales set forth there to demonstrate why Ito would not be combined with charge pump art Imamiya apply with even greater force to demonstrate why Yamashiro would not be combined with charge pump art Imamiya.

CMOS IC charge pumps have been designed since prior to the June 1974 filing date of US 3,942,047 (Buchanan). Thus, for over thirty years skilled designers have been solving every recognized problem with IC charge pumps. Every single charge pump couples a clock to a transfer capacitor coupling switch (TCCS), and a substantial fraction of them do so without conveying substantial charge to the transfer capacitor. The predictable problem of such coupling has been thoroughly solved. The fact that for over thirty years, skilled designers of CMOS ICs without exception (on the evidence of record) have <u>never</u> employed capacitors to couple a charge pump clock to a TCCS, except when such coupling is performed by the transfer capacitor itself, is compelling evidence that using capacitors for such coupling is <u>uniformly disapproved and believed undesirable by all designers</u>.

Of course such coupling is possible, or the Appellants could not have done it. It is undesirable, however, because it is significantly more expensive than using simple active circuits to achieve such coupling. Were there some reason to use capacitive coupling as claimed, were CMOS

active circuitry not vastly superior to capacitive coupling for this task, then at least one skilled CMOS IC designer in the more than thirty years of IC charge pump development would have employed capacitive coupling as claimed. The fact that the Examiner has turned to wholly nonanalogous art to demonstrate the possibility of such coupling is itself evidence underscoring the total dearth of such use in CMOS IC designs. Stated in the terms used in *W.L.Gore*, the absence of any examples of capacitive coupling in over three decades of prior art development, as exemplified in the scores patents disclosing CMOS IC charge pump designs that are of record, is strong evidence that the prior art, taken as a whole, teaches away from such coupling.

Thus, in general a person of skill in the art will not design a charge pump by following teaching of non-charge pump art in a manner that is contrary to well-developed solutions described by extensive teaching that is proven desirable for charge pumps. The obvious exception to this general rule is the case in which a designer has some particular motivation or reason to make such a change to standard practice. The Examiner suggests no such reason or motivation, and none is seen in the art. The advantage of the claimed feature deduced by the Appellants was not known, and could not easily be deduced, following as it does from the fact that a slow analog clock reduces noise, which was unknown, and that capacitive coupling becomes desirable for reasons relating to the implementation of a slow analog clock.

The rejections of specific claims as obvious over Imamiya in view of Ito and Yamashiro are addressed in the remarks set forth below. The Examiner primarily relies upon Yamashiro as evidence that one of skill in the art would use a capacitor to couple a signal to a target. But while a designer using discrete components (as in Yamashiro) would often use a discrete capacitor because it is less expensive and in many ways more powerful than active devices, in integrated circuit design the exact opposite is true: active devices are inexpensive and generally more powerful than IC capacitors. Integrated circuits, and especially CMOS ICs, can achieve most functions that would be performed by capacitors, with the notable exception of storing charge, using tiny active devices instead of large capacitors. In particular, a skilled person would not make such a modification to basic IC charge pump design conventions, as proven by the complete absence of a CMOS IC charge pump that thus employs capacitive coupling despite over thirty years of extensive and vigorous design and development in charge pumps.

VII.B.3.a Rejection of Claims 5-8 over Imamiya in view of Ito and Yamashiro

Claim 1 is nonobvious over Imamiya in view of Ito for the many reasons set forth, or incorporated by reference, in subsection *VII.B.2.d Rejection of Claims 1 and 43, plus 2-4, 10, 44-45, 48 and 68-69 over Imamiya + Ito*, incorporated here by reference. Imamiya in view of Ito fails to render obvious Claim 1 because, in abbreviated summary: 1. Imamiya and Ito fail to disclose that the output TCCS is controlled by a clock, as required; 2. there is no motivation for a skilled person to design contrary to the well established teaching of the prior art of IC charge pumps; 3. the prior art of IC charge pumps does not disclose a charge pump clock generator consisting of a three stage current starved ring oscillators having not more than (and, for Claim 68, not less than) three inverter stages; 4. Ito is not charge pump art and does not mention charge pumps, but rather is concerned with VCOs; 5. no reason is provided to suggest that the output of the Ito oscillator circuit would be suitable for charge pumps; and 6. the charge pump prior art (Hara) teaches that such oscillators, when used for charge pumps, should have at least five inverter stages. As such, under the law according, for example, to the *W.L.Gore* decision, Claims 1, 2, 5-8 and 68 are nonobvious over Imamiya, even combined with Ito, at least by virtue of either being, or properly depending from, Claim 1.

The ground of rejection addressed in this subsection differs from that of subsection *VII.B.2.d* by the addition of the Yamashiro reference. Yamashiro teaches a MISFET amplifier, which has nothing to do with charge pumps and therefore would not be followed by a skilled person to modify conventional charge pump designs. Irrespective of the fact that it is nonanalogous art, Yamashiro does not in any event include disclosure that could remedy any of the failures of Imamiya and Ito to render obvious Claim 1. Yamashiro has no teaching in regard to charge pumps, and thus cannot remedy failure 1. above; provides no motivation for combining Ito with Imamiya to remedy 2.; has no teaching relevant to 3.; has no teaching relevant to charge pumps and hence cannot remedy 4. or 5., or overcome the teaching away by charge pump prior art that is indicated in item 6. As such, the three references combined do not render obvious Claim 1 or any of Claims 2, 5-8 and 68, each of which properly depends from Claim 1.

Claims 7-8 are further distinguished over this combination of references irrespective of the nonobviousness of Claim 1. Claim 7 properly depends from Claim 6 and Claim 8 properly depends from Claim 5. Claims 5 and 6 both require at least one "capacitive coupling circuit ... to couple one of the ... charge pump clock outputs to a control node of one of the ... transfer capacitor coupling switches." The transfer capacitors C of Figure 5 of Imamiya arguably disclose the literal requirements recited by Claims 5 and 6. However, the requirements of Claims 5 and 6 are not disclosed in Figure 10 of Imamiya or the accompanying text; and no other disclosure of Imamiya is material.

However, Claims 7 and 8 both require that none of the corresponding capacitive coupling circuits is configured to conduct substantial charge to the transfer capacitor. That is contrary to the disclosure of Figure 5 of Imamiya, where the capacitors C are both transfer capacitors and coupling capacitors. In other words, each and every coupling capacitor in Figure 5 of Imamiya "conducts substantial charge to the transfer capacitor" contrary to the requirements of Claims 7 and 8.

Thus, Claims 7 and 8 both recite limitations contrary to Figure 5 of Imamiya, and incorporate limitations contrary to Figure 10 of Imamiya by virtue of depending from Claim 6 and 5, respectively. Imamiya therefore fails to disclose all of the requirements of Claims 6+7 or of Claims 5+8, irrespective of the nonobviousness of Claim 1.

The reasoned remarks set forth above in subsection *VII.B.3 Rejections as Obvious over Imamiya in view of Ito and Yamashiro* are incorporated here by reference to support a conclusion that neither Ito nor Yamashiro would be followed by a skilled person to modify a charge pump contrary to the voluminous teaching directly regarding charge pumps.

Far from being obvious, it would be absurd for a skilled person to modify the circuit of Claim 10 of Imamiya, which requires only wires to couple the clock to the TCCSs, by inserting capacitors and adding the biasing circuitry thereby required.

Figure 5 is the only other relevant disclosure of Imamiya. However, Figure 5 already discloses the use of capacitive coupling. As such, even if a designer chose to follow Yamashiro (which is denied), it is not seen that he could thereby modify the circuit of Figure 5 in any sensible manner.

Thus, it would be absurd to modify to add coupling capacitors to Figure 10 of Imamiya, and Figure 5 already discloses capacitor coupling, and as a practical matter could not be modified further for capacitive coupling. Thus, even if a skilled designer *arguendo* wanted to add capacitive coupling due to the teaching of Yamashiro, he would not do so with regard to Figure 10 because it would be absurd, and he could not do so with regard to Figure 5. Yamashiro thus cannot reasonably remedy the failures of Imamiya and Ito to arrive at the requirements of Claim 7 or Claim 8, which are accordingly nonobvious over this combination of references. For the foregoing reasons, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claims 7 and 8.

VII.B.3.b Rejection of Claims 15 and 34-35 over Imamiya in view of Ito and Yamashiro

Support for a conclusion that independent Claims 12 and 28 are nonobvious over Imamiya in view of Ito is set forth, or incorporated by reference, in subsection *VII.B.2.e Rejection of Claims 12 and 28, plus 13-14, 16, 29-33, 36 and 38-41 over Imamiya + Ito*, and all such support is incorporated here by reference.

The two most significant reasons that Imamiya and Ito fail to render obvious either of Claim 12 or Claim 28 are, first, that Ito is not charge pump art and would not be followed by a charge pump designer to modify a charge pump contrary to the long-established conventions of charge pump design without good reason, and no such reason is pointed out; and second, both Imamiya and Ito fail to even fairly suggest a "substantially sine-like" output from an oscillator, much less from a charge pump clock as required by both Claim 12 and Claim 28.

Yamashiro does not have disclosure that could remedy either of these important failures. Yamashiro has no teaching in respect of charge pumps, but is an analog amplifier designed to be fabricated using discrete components, and thus has even less in common with charge pumps than does Ito, so it would be highly nonobvious for a skilled charge pump designer to follow Yamashiro for designing an IC charge pump.

Moreover, it would be particularly nonobvious to design contrary to the clear teaching of over three decades of IC charge pump prior art development, so as to make the "significantly sine-like waveform" of Figure 5 of Yamashiro into a feature of a charge pump clock output. No

motivation or reason for such a design has been suggested by the Examiner that amounts to more than "it is possible," a contention that is itself unsupported. The expected disadvantages of using a substantially sine-like charge pump clock output waveform are indicated in remarks set forth, or incorporated by reference, in subsection *VII.A.2.a Integrated Circuit Charge Pump Clock Waveforms*, and incorporated here by reference. Such expected disadvantages are not balanced by any corresponding benefit to charge pumps from such a change that was known or reasonably expected by charge pump designers at the time of the invention.

As such, Claims 12 and 28 are, for at least those reasons, nonobvious over the references Imamiya, Ito and Yamashiro, and Claims 15 and 34-35 are therefore nonobvious over Imamiya in view of Ito and Yamashiro at least by virtue of depending from Claim 12 or Claim 28, respectively. The panel is therefore respectfully requested to reverse the Examiner's rejection of Claims 15 and 34-35 on this ground.

Claim 35, moreover, is patentably distinguished over this combination of references irrespective of distinctions due to limitations of Claims 12 and 28 from which they respectively depend. Claim 35 requires in part (underlining added for emphasis):

> The method of Claim 28, wherein actively controlled TCCS circuits each have an associated control node, the method further comprising coupling the associated control node of each of the actively controlled TCCS circuits to the first charge pump clock output via a corresponding capacitive coupling circuit.

Imamiya is the only one of the three references that includes subject matter relevant to TCCSs (transfer capacitor coupling switches). Such subject matter does not include the material that the Examiner insists on relying upon despite the Appellants' pointing out more suitable material, but does include Figures 5 and 10 of Imamiya, and the text describing those figures.

However, Figure 5 does not include <u>any</u> "actively controlled TCCS circuits" as required, and hence cannot help render obvious Claim 35. Nor does Figure 10 render Claim 35 obvious, because given that every actively controlled TCCS in Figure 10 is coupled to the clock via a simple wire, it makes absolutely no sense for an IC designer to insert a capacitor where a wire will suffice.

Accordingly, the panel is respectfully requested to reverse the Examiner's rejection of Claim 35 for the additional reasons set forth above.

VII.B.3.c Rejection of Claims 46-47 over Imamiya in view of Ito and Yamashiro

Independent Claim 43 includes limitations similar to the most important limitations of Claim1. As such, Claim 43 is nonobvious over Imamiya in view of Ito and Yamashiro for substantially the same reasons that Claim 1 is nonobvious over that combination of references. Those reasons are set forth, or incorporated by reference, in subsection *VII.B.3.a Rejection of Claims 5-8 over Imamiya in view of Ito and Yamashiro*, and are incorporated here by reference *mutatis mutandis* to support a conclusion that Claim 43 is nonobvious over Imamiya, Ito and Yamashiro. Claims 46 and 47 are accordingly nonobvious over Imamiya, Ito and Yamashiro at least by virtue of properly depending from independent Claim 43, and the panel is therefore respectfully requested to reverse the Examiner's rejection of Claims 46 and 47 on this ground.

VII.B.3.d Rejection of Independent Claim 49 over Imamiya in view of Ito and Yamashiro

The Examiner relies upon disclosure set forth in Figure 15A of Imamiya to support his contention that Imamiya in view of Ito and Yamashiro renders Claim 49 obvious. The Examiner's reliance is misplaced, and the subject matter to which he points fails to support *prima facie* obviousness of Claim 49.

Basic features of this claim include requirements for a charge pump generating an output supply from a voltage source by coupling a transfer capacitor alternately to the source and to the output. These features are not disclosed, taught or fairly suggested in either Ito or Yamashiro, nor in Figure 15A of Imamiya, upon which the Examiner relies despite the Appellants' objections to such reliance.

Ito, which describes nothing to do with charge pumps, has essentially nothing to do with Claim 49. Ito teaches oscillator details, but Claim 49 does not require oscillator details. The applicability of Ito in this rejection is therefore not understood, nor does the Examiner provide guidance. Nor is it understood what limitation of Claim 49 Yamashiro might be relied upon for, given that Yamashiro also has no charge pump teaching, and is cited elsewhere only for the concept

of capacitive signal coupling, which is not at issue in Claim 49. As such, this combination of references is no different, in effect, from a rejection as obvious over Imamiya, and it is respectfully observed that citation to Ito and Yamashiro serve only to obscure the basis of the rejection.

The remarks set forth in subsection *VII.B.1.b Rejection of Claim 49 over Imamiya in view of Pfiffner* are incorporated here by reference as relevant to this ground of rejection when "Yamashiro and/or Ito" are substituted in said remarks in place of each instance of "Pfiffner," *mutatis mutandis*.

In brief, those remarks demonstrate that Imamiya fails to disclose all the important limitations of Claim 49, particularly in respect of coupling the charge pump clock to the TC discharging switch that connects the TC to the output during discharge periods. Because neither Ito nor Yamashiro disclose any information whatsoever in respect of such charge pump switching details, they cannot, and do not, remedy the failure of Imamiya in this regard. As such, Claim 49 is nonobvious over Imamiya, even if combined with Ito and Yamashiro. As such, the panel is respectfully requested to reverse the Examiner's rejection of Claim 49 on this ground, and to particularly reverse the Examiner as to his stated rationale for rejection of Claim 49.

VII.B.3.e Rejection of Claims 54-55 over Imamiya in view of Ito and Yamashiro

Claim 54 properly depends from independent Claim 49, and Claim 55 properly depends from Claim 54.

Claim 54 requires in part (underlining added for emphasis):

> c) coupling a second TC to a second voltage source via a second TC charging switch under control of the charge pump clock output; and
> d) coupling the second TC to a second output supply via a second TC discharging switch under control of the charge pump clock output.

The Examiner's contentions in regard to Claim 54 rely upon disclosure of Imamiya that is not a charge pump and has no output supply, both of which are required by Claim 54. Because neither Ito nor Yamashiro remedy these failings, the Examiner's contentions wholly fail to support *prima facie* obviousness of Claim 49, let alone Claim 54.

However, the Appellants respectfully submit that the best rejection that could be made of Claim 49 over Imamiya would rely upon Figure 10. The Appellants respectfully submit that aside from Figures 5 and 10 and the text associated with those figures, no other disclosure of Imamiya includes details of a charge pump. Figure 5 of Imamiya is inconsistent with the requirement of Claim 49 that "a single phase charge pump clock output that is passively coupled to a control node of the TC [transfer capacitor] discharging switch and substantially isolated from the TC," because each capacitor C of Figure 5 is a transfer capacitor. Accordingly, the distinction of Claim 54 over Imamiya, Ito and Yamashiro is argued with respect to Figure 10 of Imamiya.

Figure 10 of Imamiya discloses a single input supply, V_{DD}, and a single output supply, Vout, and does not disclose either a second voltage source, or a second output supply, as required by Claim 10. All TCCSs (transfer capacitor coupling switches) coupling any TC (transfer capacitor) to an input supply couple to the same voltage source. Only one TCCS, QN73, couples a TC to the singular output supply, because all other discharging TCCSs couple TCs to other TCs, and in one instance to the input supply. Thus, Imamiya clearly fails to disclose the requirements of Claim 54, as inset above.

Neither Ito nor Yamashiro have any teaching whatsoever in respect of charge pumps, and particularly have no teaching in respect of the requirements of Claim 54 inset above. As such, they cannot remedy the failure of Imamiya to disclose the requirements of Claim 54. Consequently, the cited combination of references does not support *prima facie* obviousness of Claim 54, and the panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 54.

Claim 55 properly depends on Claim 54, and hence is nonobvious over Imamiya, Ito and Yamashiro for the reasons set forth above. Moreover, Claim 55 requires in part (underlining added for emphasis):

> [C]oupling the charge pump clock output to a control node of each TC charging switch, and to a control node of each TC discharging switch, via corresponding capacitive coupling circuits.

It would be quite absurd for a designer to employ a capacitor to couple the clock to the TC charging and discharging switches by means of a capacitor, given that Imamiya teaches using a mere direct connection for such coupling. No sensible designer would modify a design by replacing

a simple connection by an area-consuming capacitor and associated biasing circuitry that is entailed by capacitive coupling. As such, even if Yamashiro was analogous art or would be followed by a skilled designer of charge pumps, modifying Imamiya to insert a capacitor would not be obvious, but would be folly. No skilled person would make such modification. Claim 55 is accordingly distinguished over Imamiya, Ito and Yamashiro for these reasons irrespective of the nonobviousness of Claim 54 over this combination of references. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 55.

VII.B.3.f Rejection of Claims 56-59 over Imamiya, Ito, and Yamashiro

Claim 56 recites (underlining added for emphasis):

> The method of Claim 49, further comprising coupling the charge pump clock output to a control node of each actively controllable TC charging switch, and to each actively controllable TC discharging switch, via corresponding capacitive coupling circuits.

As has been frequently noted elsewhere, Imamiya is the only one of the three references cited for this ground of rejection that includes any disclosure in respect of a charge pump clock controlling transfer capacitor coupling switches (TCCSs). Ito is oscillator art and Yamashiro is discrete-component amplifier art, and neither includes any suggestion in respect of charge pumps, or any teaching of such charge pump circuits.

However, as has also been frequently noted elsewhere, Imamiya has only two sections with significant disclosure related to charge pumps; the portions of Imamiya that the Examiner insists on relying upon in his statements in support of rejections over Imamiya do not disclose a charge pump, or even a circuit having an output supply, and thus so not support *prima facie* obviousness of any pending claim of the application. The two sections of Imamiya that are relevant to charge pumps are Figures 5 and 10, plus the descriptive text respectively associated with each. Neither of these sections describes the requirements of Claim 56.

Figure 5 discloses capacitive coupling from the charge pump clock, but does not disclose any actively controllable TC charging switch, or any actively controllable TC discharging switch. Neither Ito nor Yamashiro can remedy these omissions, and the circuits of Figures 5 and 10 are far too different to be combined. Ito includes no relevant teaching whatsoever. Yamashiro is

nonanalogous art that would not be followed, particularly when no need exists in the relevant disclosure of Imamiya for capacitive signal coupling as disclosed in Yamashiro.

Figure 10 discloses actively controllable charge and discharge switches. However, for the purpose of coupling the charge pump clock to such actively controllable charge and discharge switches, no designer would replace the mere wires, taught by Imamiya, with capacitive coupling circuits. Capacitive coupling circuits require a capacitor, which occupies a great deal of IC area, and generally require a biasing circuit as well. This is vastly more difficult and expensive than simply using a wire, and no problem appears that would warrant replacing a wire with a much more expensive alternative. Thus, far from being obvious, it would be irrational to modify Imamiya Figure 10 by replacing the clock coupling, presently simple wire, by capacitors as required by Claim 56, even if it would otherwise *arguendo* be reasonable for a charge pump designer to follow nonanalogous art like Yamashiro to modify a charge pump.

But such modification would not be reasonable. That is, a skilled designer of charge pumps, having access to the teachings of over three decades of extensive prior art development specific to charge pumps, would not design contrary to the established conventions of charge pumps in order to insert a design element, capacitive coupling of a signal, that is practiced in prior art that is not directed to either ICs or to charge pumps.

In view of the foregoing, Imamiya in view of Ito and Yamashiro fails to render Claim 56 obvious. As such, the panel is respectfully requested to reverse the Examiner as to this ground of rejection of Claim 56.

Claim 57 requires in part: "[I]ncorporating circuitry to reduce voltage change rates during both positive and negative transitions of the charge pump clock output." This element is not disclosed in Yamashiro, which is not directed to clock generators or even oscillators, and is not disclosed in Imamiya, which lacks all detail in respect of the charge pump clock. As such, the ground of rejection must rely on Ito for disclosure of the element required by Claim 57.

While Ito discloses such details in the oscillator circuit of Figure 12, there is not the least suggestion that any circuit of Ito is suitable for charge pumps. In view of over three decades of development and teaching in respect of IC charge pumps showing that clocks are always square or

nearly square, it would not be obvious for skilled charge pump designer would follow teaching that is not known to be suitable for charge pumps merely to arbitrarily deviate from conventional charge pump designs. The features of Figure 12 of Ito that the Examiner relies upon would unquestionably require additional components, including capacitors that consume substantial area in an IC, which is self-evidently disadvantageous, or negatively motivated. They would unquestionably slow the clock edges, which is contrary to the practice in charge pump clock designs. Yet there is no positive motivation for such a modification. Given that Ito is not charge pump art, is not suggested to be suitable for charge pumps, and that the art of charge pumps as a whole suggests that slowing a charge pump clock is not desirable, a skilled person would not follow Ito to contravene the well-established conventions of charge pump design.

As such, Imamiya in view of Ito and Yamashiro does not render Claim 57 obvious. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 57.

Claim 58 requires in part : "[L]imiting currents output from each driver circuit of the charge pump clock generator circuit." This element is not taught by either Imamiya or Yamashiro, as noted in the remarks set forth above. For much the same reasons as set forth above, a skilled person would not follow art, such as Ito, that is not known to be suitable for charge pumps, in order to modify a conventional charge pump, in the absence of positive motivation. No such motivation is suggested. To the contrary, limiting the output current of the clock would slow the clock output, and the prior art of charge pumps taken as a whole suggests that slowing charge pump clocks is not desirable. There is thus no reason to follow non-charge pump art Ito in this regard, and there is some reason not to do so. As such, it is respectfully submitted that the absence of a showing of any motivation, including "market pressure" motivation such as relied upon in *KSR*, renders Claim 58 non-obvious over the cited combination of references. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 58.

Claim 59 properly depends from Claim 58 and is nonobvious over the cited combination of references for the reasons set forth above with respect to Claim 58. However, Claim 59 further requires "coupling a capacitor to the output node of the driver circuit." This requirement is

comparable to that of Claim 57, and as such the reasons set forth above with respect to Claim 57 are also applicable to support, irrespective of the patentability of Claim 58, a conclusion that Claim 59 is nonobvious over Imamiya, Ito and Yamashiro. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of Claim 59.

VII.B.4 Rejections as Obvious over Imamiya in view of Pfiffner and Ito

On page 18 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 20 and 22-23 as obvious under 35 USC § 103(a) over Imamiya in view of Pfiffner, and further in view of Ito.

The remarks set forth in subsection *VII.B.2.c W.L.Gore Compared to Rejections Over Imamiya / Ito and Forbes / Ito* are incorporated here by reference. Like the Markwood reference in *W.L.Gore*, both Ito and Pfiffner are secondary references that teach techniques for a different context than that of the contested claim (charge pumps). *W.L.Gore* stands for the proposition that it is nonobvious to follow the teachings of art intended for a context not encompassed by the challenged claim and not known to be useful with respect to the claim, when the prior art relevant to the claimed subject matter fails to make such suggestion, and particularly when the relevant prior art, taken as a whole, leads away from the teachings of art. The reasoning of the court in *W.L.Gore* that relevant art would not be ignored to follow art not known relevant is greatly strengthened in respect of the Appellants' claims of IC charge pumps, because IC charge pumps constitute a very crowded field that had been vigorously developed for over three decades, and had produced hundreds of patents, prior to the Appellants' invention. Thus, in the case before the panel, a skilled person has far more relevant knowledge and teaching to follow than did the inventor in *W.L.Gore*, rendering it particularly nonobvious to contradict all of such teaching, particularly in the absence of adequate motivation. Instead of adequate motivation, however, no motivation at all is suggested as a rationale for a skilled person to combine bits and pieces of various references, as proposed by the Examiner, to patch together a charge pump that is contrary to the long and well-established conventions of prior art charge pumps.

VII.B.4.a Rejection of Claims 18 and 22-23 over Imamiya, Pfiffner and Ito

Claims 18 and 22-23 properly depend from Claim 18. Remarks incorporated by reference, or set forth directly, in subsection *VII.B.1.a Rejection of Claim 18 over Imamiya and Pfiffner*, are incorporated here by reference. Said remarks amply support a conclusion that Claim 18 is nonobvious over Imamiya in view of Pfiffner. The following remarks summarize and/or complement those incorporated remarks, and extend them to address the addition of Ito for this ground of rejection. In sum, these remarks support a conclusion that Claim 18 is nonobvious over Imamiya in view of both Pfiffner and Ito.

Figure 5 of Imamiya is contrary to the requirement of Claim 18 that a charge pump clock be coupled passively "without conveying substantial transfer current" to control nodes of each of the switching devices. Claim 18 requires the clock to be coupled to a control node of each of the source switching devices and each of the output switching devices to cause conduction or nonconduction, as appropriate, to the source or output, as appropriate. But in Figure 10, the output switch QN73 is passive, and thus not controlled by coupling to the clock, as required for each output switch that causes conduction to the output. This is not a minor difference. Instead, such a passive device is essential to permit passive coupling to all other transfer capacitor coupling switches (TCCSs) without causing destructive simultaneous (or cross-) conduction through TCCSs. Thus, Figure 10 of Imamiya fails to teach all the transfer capacitor switching requirements of Claim 18.

Figures 5 and 10 have entirely different architectures. Figure 5 is an example of the first class of charge pumps, which have a "direct TC drive" clock output as described in subsection *V.D.1 Two Types of Charge Pumps*, the contents of which are incorporated here by reference. The clock outputs in Figure 5 directly provide substantially all of current into and out of the transfer capacitors. Figure 10, by contrast, is an example of the second or "control only" class of charge pumps, in which the clock merely provides control for separate transfer capacitor coupling switches (TCCSs). Due to their contrary transfer capacitor switching architectures, elements of the two cannot practically be combined or swapped between the designs. Thus, neither Figure 5 nor Figure 10 can remedy failures of the other with respect to transfer capacitor switching. Moreover, neither Ito nor

Pfiffner have any teaching whatsoever in respect of charge pump transfer capacitor switching, and thus they are likewise unable to remedy failures of either charge pump of Imamiya in this regard.

Because Ito cannot remedy the failure of Imamiya and Pfiffner to disclose transfer capacitor switching as required by Claim 18, Claims 20 and 22-23 are nonobvious over Imamiya, Pfiffner and Ito by virtue of properly depending from Claim 18. The panel is therefore respectfully requested to reverse the Examiner's rejection of Claims 20 and 22-23 on this ground.

VII.B.4.b Rejection of Claim 20 over Imamiya, Pfiffner and Ito

Irrespective of being nonobvious over Imamiya, Pfiffner and Ito for the reasons set forth in the immediately preceding subsection, Claim 20 recites an additional limitation that is not present in any of the three references. Claim 20 recites (underlining added for emphasis):

> The apparatus of Claim 18, further comprising circuitry configured to reduce voltage change rates of the charge pump clock output during both positive and negative transitions compared to an absence of such circuitry such that the charge pump clock output voltage is substantially sine-like.

Remarks in respect of a comparable requirement in Claims 12 and 28 are set forth, or incorporated by reference, in subsection *VII.B.2.e Rejection of Claims 12 and 28, plus 13-14, 16, 29-33, 36 and 38-41 over Imamiya + Ito*, all of which are incorporated here by reference in support of a conclusion that such a requirement is not taught, disclosed or fairly suggested by Imamiya even combined with Ito.

Pfiffner is a sample and hold signal level comparator, which has essentially nothing to do with charge pumps, and thus is nonanalogous art that would not be followed by a charge pump designer, especially in view of the wealth of prior art directly relevant to IC charge pumps that had been developed over a period of more than three decades preceding the Appellants' invention.

Even were Pfiffner relevant prior art, it has no disclosure whatsoever relevant to the requirement of Claim 20 noted above, and thus cannot remedy the failure of the combination of Imamiya and Ito to render obvious Claim 20. As such, Claim 20 is nonobvious over Imamiya, Pfiffner and Ito, and the panel is therefore respectfully requested to reverse the Examiner's rejection of Claim 20 on this ground.

VII.B.5 Rejections as Obvious over Imamiya in view of Yamashiro

On page 20 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 24-25, 27, 60-61 and 66-67 as obvious under 35 USC § 103(a) over Imamiya in view of Yamashiro.

Before setting forth the many reasons why no skilled person would modify a charge pump to incorporate features set forth in the unrelated art of Yamashiro, the following remarks demonstrate that no disclosure of Imamiya would rationally be modified by following Yamashiro to result in a charge pump having an output voltage and capacitive coupling from the charge pump clock to a control node of a TC (transfer capacitor) coupling switch that is isolated from the TC.

VII.B.5.a Imamiya Cannot Be Sensibly Modified To Achieve the Claimed Invention

The portions of Imamiya that the Examiner relies upon in his rejection, Figure 15A, do not disclose all the important limitations of any of the above-noted claims because Figure 15A of Imamiya is not a charge pump, as required, and does not produce and output supply, as required. Remarks in this regard that are set forth, or incorporated by reference, in subsection *VII.B.1 Rejections as Obvious over Imamiya in view of Pfiffner* are incorporated here by reference to provide thorough support for this contention. Because the disclosure relied upon in the Examiner's statement of support wholly fails to support *prima facie* obviousness of any of the claims rejected on this ground, the Appellants address more relevant disclosure in Imamiya in remarks set forth below.

Imamiya discloses charge pumps having output supplies in Figures 5 and 10. Figure 5 illustrates a charge pump of the first class "direct TC drive" of charge pumps, as described in the remarks set forth in subsection *V.D.1 Two Types of Charge Pumps*, which are incorporated here by reference. In Figure 5 of Imamiya the charge pump clocks provide transfer current to the charge pump output via the transfer capacitor, which is connected directly to the output of the charge pump clock. The TC switching devices are FETs configured as diodes, whereby their control nodes are connected directly to the TCs. This class of charge pumps, and Figure 5 of Imamiya in particular, is contrary to a requirement of independent Claim 24 of a "control node that is substantially isolated from both the transfer capacitor and the [source or output]." It is contrary to the requirement of independent Claim 60 (a) and (c), of a first and a second "capacitive coupling network that does not

conduct a significant portion of the charge for the output." Thus, Figure 5 does not comport with the requirements of any of these claims, each of which includes all the limitations of Claim 24 or of Claim 60.

The only remaining charge pump teaching of Imamiya is Figure 10. There, the clock is coupled to transfer capacitor coupling switches (TCCSs) by means of a simple wire. To modify Imamiya to result in the invention claimed by Claim 24 or Claim 60, an IC charge pump designer would have to replace a wire or simple metal connection by a capacitor. The absurdity of this is quite clear. For one thing, capacitors require a great deal of IC area. While it would clearly be disadvantageous to make such a modification, no corresponding advantage to such coupling can be seen.

Thus, no charge pump circuits described in Imamiya could sensibly be modified to result in the claimed invention as defined in the independent claims, even if Yamashiro was prior art that a charge pump designer would follow in deviating from the extensive teaching of charge pump prior art.

VII.B.5.b Charge Pumps Would Not Be Modified According to Yamashiro

The Appellants object generally that rejections of charge pump claims over Yamashiro is inappropriate because Yamashiro is nonanalogous art, in that it would not be obvious to modify a charge pump to have a feature of Yamashiro if such feature is contrary to the cited charge pump art.

Remarks set forth, or incorporated by reference, in subsections *VII.B.3 Rejections as Obvious over Imamiya in view of Ito and Yamashiro* and *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito* are incorporated here by reference because, applied *mutatis mutandis*, the rationales set forth there to demonstrate why Ito would not be combined with charge pump art Imamiya apply with even greater force to demonstrate why Yamashiro would not be combined with charge pump art Imamiya.

Yamashiro does not disclose a charge pump, or even an oscillator, but a linear amplifier fabricated from discrete components. It has very little in common with the subject of the invention, aside from using the most basic library of electronic components, including resistors, capacitors, and

transistors. The transistors are FETs, but not MOSFETs on an IC, but discrete MISFETs. There is no common problem, no reason whatsoever for a skilled person to turn to such art to modify a charge pump.

For all of the reasons set forth above, it is nonobvious to modify an IC charge pump of the "control only" type (as described in subsection *V.D.1 Two Types of Charge Pumps*) in accordance with the non-IC, non-charge pump art of Yamashiro, to arrive at an IC charge pump that is contrary to over thirty years of contrary IC charge pump prior art designs.

VII.B.5.c Rejection of Claims 24 and 60-61 over Imamiya in view of Yamashiro

The remarks set forth or incorporated by reference above in subsections *VII.B.5 Rejections as Obvious over Imamiya in view of Yamashiro*, *VII.B.5.a Imamiya Cannot Be Sensibly Modified To Achieve the Claimed Invention*, and *VII.B.5.b Charge Pumps Would Not Be Modified According to Yamashiro*, are all incorporated here by reference. These remarks include a multiplicity of reasons supporting a conclusion that it would not be obvious to modify any charge pump in accordance with Yamashiro to include a "capacitive clock output coupling" feature, and a further conclusion that it would be particularly nonobvious to modify a charge pump of Imamiya in such manner. As set forth in the incorporated remarks, the specific combination with Imamiya fails to render obvious either Claim 24 or Claim 60 because only Figures 5 and 10 of Imamiya are charge pumps as claimed, Figure 5 is contrary to requirements of both claims, and it would be absurd to modify the circuit of Figure 10 to replace the simple wire coupling there with a capacitive coupling circuit, as required. Also, because the circuits of Figures 5 and 10 are examples of different classes of charge pumps that operate very differently, as explained in remarks set forth in subsection *V.D.1 Two Types of Charge Pumps*, it is not possible to "mix and match" features between the two Figures.

For all the reasons set forth or incorporated by reference above, Claims 24 and 60 are nonobvious over a combination of Imamiya and Yamashiro. For purposes of this rejection only, Claim 61 may stand or fall with Claim 60 from which it depends. In view of the foregoing, the panel is respectfully requested to reverse the Examiner's rejection of Claims 24, 60 and 61 on this ground.

VII.B.5.d Rejection of Claims 25, 27 and 66-67 over Imamiya in view of Yamashiro

Each of Claims 25, 27 and 66-67 require additional instances of capacitive coupling of clock outputs to switch control nodes compared to that required by Claims 24 and 60. The increase in number of capacitive coupling circuits required further distinguishes these claims over independent Claims 24 and 60 from which they depend. In particular, the additional requirement at least doubles the absurdity of replacing a wire by a capacitive coupling circuit, as proposed by the Examiner.

Irrespective of the nonobviousness of Claims 24 or 60 from which they depend, the panel is therefore respectfully requested to reverse the Examiner's rejection of Claims 25, 27 and 66-67 for this further reason.

VII.B.6 Rejections as Obvious over Forbes in view of Ito

On page 23 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 1-2, 4, 9-10, 12-14, 16-17, 28-33, 36-41, 43-45 and 68-69 as obvious under 35 USC § 103(a) over Forbes in view of Ito.

VII.B.6.a Rejection of Claims 1-2, 4, 43-45 and 68-69 over Forbes in view of Ito

Forbes suggests no detail or circuitry whatsoever for the charge pump clocks, let alone the feature details required by Claims 1 or 43. As such, the examiner turns to other prior art to demonstrate that three (or less) stage ring oscillators are known for use with charge pumps. Unfortunately, no charge pump prior art of record teaches, discloses, or fairly suggests such a charge pump oscillator. The examiner therefore turns to non-charge pump prior art, Ito. This is inappropriate for reasons described by remarks set forth, or incorporated by reference, in subsections *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*, and *VII.B.2.c W.L.Gore Compared to Rejections Over Imamiya / Ito and Forbes / Ito*, all of which are incorporated here by reference.

Those incorporated remarks, modified *mutatis mutandis*, for example to replace references to Imamiya by reference to Forbes where practical, amply demonstrate: 1) that Ito is not charge pump art that a skilled person would follow to modify a charge pump contrary to the teachings of the large body of IC charge pump teaching developed over more than thirty years; and 2) that in particular, Ito

would not be followed under the law of *W.L.Gore* to modify a charge pump to use a current starved ring oscillator having not more than three sections, as required by Claims 1 and 43, because it is not taught anywhere in charge pump art and, to the contrary, charge pump art as a whole, including the Hara reference, previously cited by the Examiner, teaches away from those limitations.

Forbes, like Imamiya, provides no information about circuitry to produce a clock signal, so for all clock signal generation, the Examiner relies upon his unwarranted conclusion that it would have been obvious for a skilled person designing a charge pump to follow Ito, contrary to the entire body of the large and crowded field of charge pump prior art developed during a period of over three decades. Part of the Appellants' response to the Examiner's comparable previous rejection is inset below as apposite (Amendment After Reopening Prosecution, last paragraph on page 26, underlining added for emphasis):

> As noted elsewhere, three stage current starved ring oscillators are a fine choice for a VCO, which can tolerate and may even desire a sine-like oscillator output. However, no charge pump prior art of record suggests having slow, sine-like clock outputs, or using three stage ring oscillators for charge pumps. To the contrary, all of the numerous charge pump references of record that address this issue show a fast-edged clock signal that would be produced by charge pumps having more stages. Moreover, the only charge pump prior art reference addressing the issue of the number of stages, Hara, expressly suggests that at least five stages should be used with charge pumps. <u>The nonanalogous prior art of Ito would not be followed, in view of the abundant evidence in this crowded field of art that teaches, both by implication from the absence of a suggestion for three stage ring oscillators and by express contrary suggestion, that three stage ring oscillators were thought unsuitable for use in charge pumps</u>. As such, the three stage current starved ring oscillator required by Claims 1 and 43 is nonobvious over the charge-pump prior art of record. The examiner is therefore respectfully requested to withdraw this ground of rejection as to independent Claims 1 and 43, and as to all claims properly depending therefrom, including Claims 2, 4, 9-10, and 44-45.

The remarks incorporated by reference above include a demonstration that the present facts are comparable to those upon which the court in *W.L.Gore* found the claims nonobvious. The demonstration is as readily applied to the present rejection over Forbes in view of Ito as over the rejection over Imamiya in view of Ito, the context in which they were originally set forth.

The reasoning set forth or incorporated by reference above amply demonstrates that Claims 1 and 43 are nonobvious over Forbes in view of Ito, and the panel is therefore respectfully requested to

reverse the Examiner's rejection of Claims 1 and 43 on this ground. As to this ground of rejection only, Claims 2, 4, 44-45 and 68-69 may stand or fall with Claim 1 or Claim 43 from which they depend.

VII.B.6.b Rejection of Claim 10 over Forbes in view of Ito

Claim 10 is nonobvious over Forbes in view of Ito by virtue of depending from Claim 1, for all the reasons set forth, or incorporated by reference, in subsection *VII.B.6.a Rejection of Claims 1-2, 4, 43-45 and 68-69 over Forbes in view of Ito*, above.

Claim 10 is nonobvious over Forbes in view of Ito, irrespective of the nonobviousness of Claim 1, because both Forbes and Ito fail to disclose the requirements recited by Claim 10. In particular, Claim 10 requires in part: "[C]oupling substantial charge into the transfer capacitor via the charge pump clock output." Claim 10 makes clear that Claim 1 covers charge pumps of both "control only" and "direct TC drive" types, as set forth in subsection *V.D.1 Two Types of Charge Pumps*. Ito does not disclose any type of charge pump. Forbes does not disclose any charge pumps, such as those of the "direct TC drive" type, having a charge pump clock output that couples substantial current into a TC.

The Examiner's statement in support of this ground of rejection seems to misunderstand the requirement that the charge be coupled into the TC via the charge pump output. He asserts "with the conducting state controlled by output Ø, the charge will be via charge pump clock output Ø, thus rendering claim 10 obvious." The Examiner finally rejected this claim without comment, after requesting explanation of the meaning of the phrase in his Office Action issued May 17, 2007, which the Appellants helpfully provided (Response mailed September 17, 2007, page 15, penultimate paragraph, underlining in original):

> The Examiner requests clarification of what is meant by "coupling substantial charge into the transfer capacitor via the charge pump clock input" as recited in Claim 10. The Applicant is pleased to provide such explanation, because two important topographies of charge pumps are distinguished from each other by their differences in this regard. The quoted language indicates that, in embodiments covered by Claim 10, (substantial) charge actually comes from the charge pump clock itself. In Figure 6 of the subject application, clock input CLK 524 does NOT couple substantial charge into the transfer capacitor. There may be a small amount coupled, in that embodiment, via the parasitic gate capacitances of the coupling switches 602,

> 604, 608 and/or 610, but it would not be substantial. In Figure 6, the primary conduction path for the transfer capacitor 606 is via the channels of said coupling switches, NOT via the clock input. Thus, Claim 10 does not read on the circuit of Figure 6. By contrast, Figure 7 illustrates an example of other embodiments described in the subject application, in which the current coupled into transfer capacitor 702 via the clock input CLK 524 is very substantial, indeed including all of such current; Claim 10 may read on such embodiments. Claim 10 thus underscores that embodiments described by Claim 1, which do not contain this limitation, may have either of these two distinct topologies.

The remarks set forth in subsection *V.D.1 Two Types of Charge Pumps* are incorporated here by reference to provide further understanding in this regard.

The first definition of "via" is as follows: 1. by a route that touches or passes through; by way of: *to fly to Japan via the North Pole.* ("Webster's Encyclopedic Unabridged Dictionary of the English Language" © 1989 by dilithium Press, Ltd.) Another dictionary has only one definition of "via": By way of. ("The American Heritage Dictionary of the English Language," © 1979 by Houghton Mifflin Company) The Appellants intend and adopt these compatible definitions. Because no term is likely to be absolutely free from ambiguity, construction of the meaning will inevitably require resort to the vast prosecution history of this application. As such, the Appellants' chosen meaning is controlling.

Because neither Forbes nor Ito fairly suggests the requirements set forth in Claim 10, the panel is respectfully requested to reverse the Examiner's rejection of Claim 10 on this ground.

VII.B.6.c Rejection of Claims 12-14, 16, 28-30, 33, 36, 38 and 40-41 over Forbes in view of Ito

A primary limitation of both Claims 12 and 28 is for a charge pump clock output that is "substantially sine-like." Neither Forbes nor Ito provide any suggestion of a waveform that is somewhat sine-like, let alone substantially sine-like. The Examiner does not contend that either reference includes any such suggestion. Instead, he points out features of Ito that will cause the oscillator (which is not a charge pump clock) output in Ito to be less than a perfect square wave. The Appellants cannot disagree, because perfect sine waves may be nearly impossible to create, but perfect square waves are physically impossible to create, and thus every real square wave is imperfect. He then asserts casually, supported by no evidence whatsoever, that any waveform that is not perfectly square is "substantially sine-like." This reasoning can be readily deduced from the

Examiner's statement supporting this aspect of the rejection of Claim 12 over Forbes in view of Ito (Office Action issued December 12, 2007, page 25 lines 16-18, underlining added for emphasis):

> The periodic switching of 488-489 and 491-492 will be provided by a waveform that is substantially sine-like (e.g. not a true square wave) due to the current limiting of Ito's 61 and 64, and capacitance 53c.

With all due respect, this is not an obviousness rejection but a clarity rejection: the Examiner effectively contends that "substantially sine-like" means any alternating waveform, because no real waveform is a "true square wave," and thus "not a true square wave" encompasses all real waveforms.

The Appellants respectfully submit that a waveform that is "substantially sine-like" means, as its terms suggest, a waveform that is substantially like a sine wave. A sine wave is a mathematical ideal that describes a particular functional relationship between voltage amplitudes at different parts of the waveform. It may be scaled in time, amplitude and average value, but is otherwise a function that allows no tolerance for real life variations.

A signal that is "substantially sine-like" has a waveform with a significantly sine-like shape, that is, it is much like a sine wave, but need not have a precise sine wave shape. A narrower definition is not needed. There is no suggestion in thirty years of IC charge pump prior art of an IC charge pump clock output waveform that is not more like other waveforms, such as triangular, sawtooth, trapezoidal, or especially square, than like a sine waveform. As such, no waveform identified within the extensively developed prior art is even close to the specified limitation.

The definition of "sine wave" is an infinitely narrow, precise mathematical function. A waveform that is "substantially like" a precise mathematical function is not, merely because of the term "substantially," effectively undefined, contrary to the Examiner's explicit position (in rejections under 35 USC 112) and implicit position (as presently). To the contrary, courts have repeatedly held that the broadening term "substantially" is perfectly acceptable, and does not render the subject matter indefinite (*see, e.g., Andrew Corp. v. Gabriel Electronics,* 847 F.2d 819, 822, 6 USPQ2d 2010 (Fed. Cir. 1988)).

Perhaps expert testimony is needed to the effect that one of skill in the art would readily understand "substantially sine-like" to describe a waveform that is more like a sine wave than like any other well-known waveform, such as a square wave, triangular or sawtooth wave. However, the Examiner is unable to point to any actual waveform, despite the numerous examples set forth in the voluminous prior art of IC charge pumps, that even passes the "red face" test as reasonably being asserted to be "substantially sine-like."

The Examiner's reliance on Ito for a "substantially sine-like" waveform is improper for two reasons. First, as noted above, Ito does not disclose or fairly suggest an oscillator output that is "substantially sine-like." However, waveforms that are nearly perfect sinusoids are produced by many oscillators. The Examiner should have been readily able to locate such an oscillator to cite as a basis for asserting that Claims 12 and 28 are obvious. Any such oscillator, however, would have the same problem as Ito: the Examiner has found no reason whatsoever why a skilled IC charge pump designer would modify an IC charge pump design contrary to all IC charge pump examples seen within IC charge pump prior art designs developed over the course of more than three decades. Or, at least, the Examiner has not pointed to any such motivation in support of his assertions of obviousness.

This ground of rejection fails to disclose important limitations required by Claims 12 and 28, in particular the requirement for a charge pump clock output that is "substantially sine-like," rendering Claims 12 and 28 nonobvious over Forbes and Ito. The Examiner's assertion that any waveform that is not a true square wave is, therefore, "substantially sine-like" is contrary to the common understanding of anyone of modest skill in the electronic arts.

The Examiner's contention that virtually any time varying waveform is a substantially sine-like waveform is untrue, and exceedingly unhelpful. MPEP 2173.06 states that a rejection over prior art is improper if uncertainty as to a term is great, and is helpful only when the degree of uncertainty is small. The degree of uncertainty should be small to a reasonable examiner, but if the Examiner refuses to grant any reasonable meaning to "substantially sine-like" then rejections over the prior art are simply a large waste of time and resources.

Even were the Examiner's extraordinarily overbroad construction of "substantially sine-like" reasonable, his reliance on Ito for this limitation would still be misplaced because Ito sets forth no teaching about waveforms, and even further, any teaching in nonanalogous art Ito in respect of waveforms would not be applicable to charge pumps. The Examiner fails to demonstrate even a remotely plausible example of, or suggestion for, using a "substantially sine-like" clock waveform in a charge pump. Claims 12 and 28 are nonobvious over the combination of Forbes and Ito for this further reason.

The reasons set forth or incorporated by reference above amply support a conclusion that Claims 12 and 28 are nonobvious over a combination of Forbes and Ito. Accordingly, the panel is respectfully requested to reverse the Examiner's rejection of Claims 12 and 28 on this ground. For purposes of this rejection only, Claims 13-14, 16, 29-30, 33, 36, 38 and 40-41 may stand or fall with Claim 12 or Claim 28, from which they depend.

VII.B.6.d Rejection of Claims 9, 17, 37 and 39 over Forbes in view of Ito

Claim 9 is nonobvious over Forbes in view of Ito by virtue of depending from Claim 1, for all the reasons set forth, or incorporated by reference, in subsection *VII.B.6.a Rejection of Claims 1-2, 4 and 43-45 over Forbes in view of Ito*, above.

Claim 9 further requires in part: "wherein the active current limit circuitry of (c)(i) and (c)(ii) is further configured to limit source and sink currents, conducted by each driver section within the charge pump clock generating circuit, to substantially identical magnitudes." Imamiya discloses no details in respect of charge pump clock generation, and Ito does not disclose, teach or fairly suggest the requirements set forth in Claim 9.

In regard to this ground of rejection of Claim 9, the Examiner points (Office Action issued December 12, 2007, page 24 from last full sentence) to "The current mirror configurations shown in Ito's Fig. 12." He points out correctly (underlining added for emphasis) "the sink currents through transistors 62-64 will correspond to the currents flowing within transistors 56-57," and continues "the source currents through transistors 59-61 will correspond to the current flowing within transistor 58. With transistors 58 and 57 coupled in series between Vdd and Vss, their currents will be the

same." The Examiner's assertions are literally correct, but they do not lead to his conclusion that Ito suggests the source and sink currents will have substantially identical magnitudes. Ito expressly teaches, to the contrary (Ito, col. 2 lines 16-28, specifically lines 25-28, underlining added for emphasis): "[I]nto the N-channel transistors 62, 63 and 64 for current controlling, there flow currents proportional to respective size ratios of the transistors 62, 63 and 64 to the transistor 57 (or the transistor 56)," and similarly with respect to the source current limiting transistors. Thus, Ito not only fails to suggest that the currents should have identical magnitude, but expressly points out that the magnitudes may be different in each case, depending on the relative sizes of the transistors. Ito does not suggest any particular relative sizes for the transistors in question, or otherwise suggest one or more particular current ratios.

Claims 17, 37 and 39 are nonobvious over Forbes in view of Ito for all of the reasons set forth, or incorporated by reference, in subsection *VII.B.6.c Rejection of Claims 12-14, 16, 28-30, 33, 36, 38 and 40-41* over Forbes in view of Ito, above.

The Examiner supports his rejection of Claim 17 (Office Action issued December 12, 2007, page 26, lines 10-12) only by referencing his arguments with respect to Claim 9, and supports his rejection of Claim 37 with reasons (Office Action issued December 12, 2007, page 27, lines 13-15) that are a subset of those he sets forth with respect to Claim 9. As such, in view of the fact that Claims 17 and 37 set forth similar requirements as Claim 9, Claims 17 and 37 are additionally nonobvious over their respective independent claims for the reasons set forth in the preceding paragraph. Claim 39 properly depends from Claim 37, and is accordingly nonobvious over Forbes in view of Ito for the same set of reasons.

Because Ito (as well as Imamiya) fails to suggest the requirements set forth in any of Claims 9, 17 or 37, but instead teaches to the contrary, these claims are each additionally nonobvious over their respective independent claims for the reasons set forth above. The panel is therefore respectfully requested to reverse the Examiner as to this ground of rejection of each of Claims 9, 17, 37 and 39.

VII.B.6.e Rejection of Claim 32 over Forbes in view of Ito

Claim 32 is nonobvious over Forbes in view of Ito by virtue of properly depending from each of Claims 31, 30, 29 and 28, for all the reasons set forth or incorporated by reference in subsection *VII.B.6.c Rejection of Claims 12-14, 16, 28-30, 33, 36, 38 and 40-41 over Forbes in view of Ito.* Claim 32 is also nonobvious over Forbes in view of Ito, irrespective of the nonobviousness of Claims 28-31, for the reasons indicated below.

Claim 32 requires in part: "[C]oupling the TC to a connection of the source voltage during a charging period via the charge pump clock output." Remarks set forth above in subsection *VII.B.6.b Rejection of Claim 10 over Forbes in view of Ito* are incorporated here by reference, particularly for their teaching in respect of the meaning of "via." As noted in the incorporated remarks, "via" is properly understood to mean "by a route that touches or passes through; by way of," or simply "by way of."

Ito does not describe charge pumps at all, and hence has no disclosure relevant to the limitations set forth in Claim 32. Forbes also fails to disclose those limitations. The Examiner asserts (Office Action issued December 12, 2007, page 27, lines 5-7) that TC 412 is connected to source voltage 402 during the charging period via charge pump clock output Ø, when TCCS circuit 489 is conducting. TCCS 489 appears only in Figure 8 of Forbes; and while it is *controlled* by clock output Ø, no conduction between the TC and the source voltage occurs via the clock output, as via is properly understood. Accordingly, the Examiner is mistaken, and Forbes does not teach, disclose or fairly suggest the limitations set forth in Claim 32. Because Ito has no relevant disclosure and cannot remedy this omission by Forbes, the combination of Forbes and Ito does not support *prima facie* obviousness of Claim 32, which is therefore nonobvious over Forbes in view of Ito. As such, the panel is respectfully requested to reverse the Examiner's rejection of Claim 32 on this ground.

VII.B.7 Rejections as Obvious over Tasdighi in view of Yamauchi

On page 29 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 1-4, 10, 12, 14, 16, 43-44, 48, 50-51, 53, 57-58 and 68-69 as obvious under 35 USC § 103(a) over Tasdighi in view of Yamauchi.

Independent Claims 1 and 43 are significantly distinguished by requiring a ring oscillator of not more than three inverter stages. Tasdighi discloses no oscillator details at all, and Yamauchi, contrary to the Examiner's contention, makes no suggestion as to a magnitude of the number of inverter stages. The Examiner relies on Figures 6 and 7 of Yamauchi, which clearly indicate omitted repetitive material. The Examiner incorrectly concludes that a three stage current starved ring oscillator is illustrated or suggested, when the illustrations imply more than three stages, and at best illustrate precisely what the text states: "an odd number of inverter stages."

Independent Claim 12 is significantly distinguished by a requirement of a charge pump clock that produces a "substantially sine-like" output. Neither Tasdighi nor Yamauchi contains the least hint that a charge pump clock output waveform should be anything other than square or "pulse."

Although not rejecting independent Claim 49 on this ground, the Examiner rejects Claims 50-51, 53 and 57-58 that depend from Claim 49. However, the stated grounds fail to render even Claim 49 obvious. Claim 49 requires specific features in the coupling between the charge pump clock and the switches that control conduction to the transfer capacitor (TC). Neither Tasdighi nor Yamauchi illustrates such features, nor indeed <u>any</u> features of such coupling, instead showing only an arrow (a non-electrical symbol) that points from the clock to the charge pump circuit to indicate that control is asserted. As he has persisted in doing for years despite the vehement protests of the Appellants, the Examiner asserts that the claim is rendered obvious because Tasdighi and Yamauchi contain nothing that would preclude the features as claimed. The Examiner's logic is so contrary to law and normal practice that the Appellants are nearly rendered speechless. A blank sheet of paper, according to that logic, renders every possible claim obvious, because it contains nothing that would preclude it from containing the information specified in any of such claims.

Every other rejected claim depends from one of independent Claims 1, 43, 12 or 49. Detailed arguments are set forth below.

<u>VII.B.7.a Rejection of Claims 1-2, 43-44 and 68-69 over Tasdighi in view of Yamauchi</u>

Claim 1, as presently pending, recites in part (underlining added for emphasis):

> c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of not more than three inverting driver sections cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches, and wherein each driver section includes
>
> i) circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output, and
>
> ii) circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output

Neither reference suggests the underlined limitation. The Examiner acknowledges that Tasdighi fails to disclose the underlined limitations, stating (Office Action of December 12, 2007, sentence bridging pages 29-30): "However, the Tasdighi reference does not clearly show or disclose charge pump clock generating circuit 2 comprising a ring oscillator with no more than three inverting driver sections, or circuitry for limiting current at a driver section's output." Thus, the Examiner relies upon Yamauchi to disclose these elements of Claim 1 as set forth above. In so doing, the Examiner states (Office Action of December 12, 2007, page 30 lines 4-8) that Figs 6 and 7 of Yamauchi show examples of a ring oscillator, "wherein each figure shows it comprising at least three inverter driver sections," and also that "Yamauchi provides support for the use of controlling a charge pump with a ring oscillator with an odd number of driver sections, which includes three sections."

The limitation in Claim 1 to "not more than three" inverter stages is very explicit, and is not suggested by a mere observation that a ring oscillator should have "an odd number" of stages. In respect to the number of inverter stages in a ring oscillator for a charge pump, Yamauchi sets forth the following: (col. 10 lines 23-24) "Referring to Fig. 6, ring oscillator 39 is formed having an odd number of inverters connected in series." The same description of the number of inverter devices as simply "odd" is repeated elsewhere (*e.g.*, col. 10 lines 37-40 and col. 11 lines 48-51). There is no teaching or suggestion whatsoever of a limitation as to the magnitude of the number of inverter sections. Thus, Yamauchi suggests the functional requirement of an odd number, but suggests no limitation on the magnitude of the number of inverters in a ring oscillator for a charge pump.

The prior art of charge pumps often refers to a ring oscillator requiring an "odd number" of stages, because an odd number of stages is a necessary condition for oscillation in conventional ring oscillators. Conventional ring oscillators also require a minimum of three inverter stages to form a ring having "an odd number" of inverters.

Figures 6 and 7 of Yamauchi are clearly abbreviated illustrations that show only the minimum number of inverter stages necessary to establish their connection pattern in a ring oscillator. The existence of additional instances of inverter sections is implied, as represented by groups of three dots replacing relevant connection lines. The three dot groups indicate that repetitive material has been omitted from the illustration. The implication is therefore that additional driver sections are ordinarily included, but have been omitted from the drawing (*e.g.*, to avoid obscuring detail). As such, the most natural implication of these figures is that they represent ring oscillators having more than three inverter stages. Even if the illustrations are not interpreted as expressly excluding a current starved ring oscillator having only three stages, they certainly do not suggest any limitation on the magnitude of the number of inverters. They thus illustrate, at most, precisely what the associated text describes: a ring oscillator having "an odd number of inverters," with no suggestion as to a magnitude for the number of inverters. If there is any magnitude implication in the figures, it is that there are "more than three" inverter stages.

Yamauchi is silent as to the magnitude of the number of inverters of the ring oscillators of Figures 6 and 7, but the waveform described by Yamauchi is incompatible with very short current starved ring oscillators (*e.g.*, having only three stages). The only disclosure seen in Yamauchi in respect of the waveform of the clock signal is as follows (emphasis added): "The oscillation circuit oscillates a pulse voltage ... ," (col. 3 line 51); "the frequency of the pulse voltage becomes lower ..." (col. 3 line 58); and "clock signal (pulse voltage) CLK ..." (col. 10 line 13). There is nothing in Yamauchi to suggest that the term "pulse voltage," particularly in this context of a repetitive pulse voltage, has any other than its usual meaning of a rectangular wave. Detailed remarks set forth in subsection *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*, particularly subheading *A 3-Stage Current Starved Ring Oscillator Generates Undesirably Slow Output Waveform*, are incorporated here by reference to support a conclusion that the waveform described by Yamauchi (pulse) is incompatible with a very short current starved ring oscillator,

particularly one of only three stages, which would tend to have a distinctly unsquare waveform. The incorporated remarks also provide technical reasons that slow-edged clock waveforms are undesirable in conventional IC charge pumps.

The foregoing remarks demonstrate that Yamauchi includes either no suggestion whatsoever that a ring oscillator for a charge pump should be limited to not more than three inverter stages, as required by Claim 1, or a suggestion that there should be more than three inverter stages. Moreover, the implication in Yamauchi, taken as a whole including the waveform description, actually suggests that a three stage current starved ring oscillator would in fact be unsuitable for the waveform expectations expressed in Yamauchi.

Prior Art As A Whole Teaches Away From Three Stage Current Starved Ring Oscillators: As noted elsewhere, *W.L.Gore* stands for the proposition that the teaching of the prior art as a whole must be considered in determining whether or not a particular magnitude limitation is suggested. In *W.L.Gore*, the primary reference was silent as to a magnitude limitation, and the secondary reference supplied the magnitude limitation, but in a somewhat different context. Here, unlike in *W.L.Gore*, not only the primary reference but also the secondary reference is silent as to the magnitude limitation. In *W.L.Gore*, the "teaching away" from the claimed combination by the prior art as a whole buttressed a conclusion that a magnitude limitation in prior art having an incompatible context did not render obvious the claimed combination, including the magnitude limitation. The present ground of rejection does not include a reference (such as Ito) that suggests the magnitude limitation but in a different context. However, the fact that the charge pump prior art as a whole teaches away from the claimed magnitude limitation still buttresses a conclusion that Yamauchi cannot be properly construed as suggesting a magnitude limitation, particularly a limitation to "not more than three" inverter stages.

The prior art as a whole teaches away from a ring oscillator being restricted to having not more than three inverter stages for the following reasons. First, thirty years of extensive IC charge pump development, in which current starved ring oscillators frequently generate the clock signal for IC charge pumps, has failed (so far as can be seen) to produce a single instance of a charge pump design actually using, or even clearly suggesting, such an oscillator using only three inverter stages;

res ipsa loquitur, these facts loudly support a contention that IC charge pump designers have persistently avoided three stage current starved ring oscillators, particularly in view of the fact that ring oscillators are the most common oscillators suggested in the charge pump prior art. Second, for reasons noted and incorporated by reference above, slow-edged clock waveforms are undesirable for use in IC charge pumps; and because a very short ring oscillator would generate a slow-edged output, a very short ring oscillator is undesirable for this reason as well, a technical reason that supports the implication of the absence of such a feature in the extensive prior art. Finally, the Hara reference expressly suggests that only ring oscillators having five or more inverter stages should be employed with a charge pump (Hara, col. 5 lines 60-62). Hara is the only known charge pump prior art reference that suggests a magnitude limitation on the number of inverters in a ring oscillator for a charge pump, and the suggestion it sets forth is diametrically opposite to the three inverter stage feature that is preferred and claimed by the Appellants. Against all the above-noted implicit and explicit teaching away from a three stage current starved ring oscillator by the prior art as a whole, the Examiner points only to Yamauchi. But Yamauchi, fairly viewed, makes no suggestion of a magnitude limit on the number of inverter stages, and especially makes no suggestion of a magnitude limited to "not more than three" inverters, as required by Claim 1.

For all of the reasons set forth above, Claim 1 is nonobvious over Tasdighi in view of Yamauchi. Claim 43 has similar limitations as Claim 1, and thus identical reasoning as set forth above with respect to Claim 1 applies to support a conclusion that Claim 43 is nonobvious over Tasdighi in view of Yamauchi. The panel is therefore requested to reverse the Examiner's rejection over Tasdighi in view of Yamauchi of Claims 1 and 43, and also to reverse the rejection of Claims 2, 44 and 68-69, which, for purposes of this ground of rejection alone, may stand or fall together with either Claim 1 or Claim 43, from which they properly depend.

VII.B.7.b Rejection of Claims 3-4, 10 and 48 over Tasdighi in view of Yamauchi

Each of Claims 3-4, 10 and 48 properly depends from one of the claims addressed in the preceding subsection, and is nonobvious over Tasdighi and Yamauchi at least for that reason. Moreover, each of these claims is nonobvious over that combination of prior art for additional reasons, irrespective of the nonobviousness of Claims 1-2, 43-44 and 68-69.

Claim 3 recites in part (underlining added for emphasis): "[C]oupling circuitry configured to couple the particular charge pump clock output as a signal to each of the transfer capacitor coupling switches without increasing a rate of voltage rise or fall of the signal." Claims 4 and 48 each have a comparable limitation. This feature is significant for reducing noise generation because it is best if not only the clock signal as initially generated, but also as it is propagated to the switches it controls, is limited as to the speed (or dv/dt) of the signal. As has been repeatedly noted elsewhere, ICs, and especially CMOS ICs, have great power for processing digital signals due to the availability of extremely small active devices. As such, market pressure to employ the most efficient processing drives IC designers to employ their very powerful active devices to couple a clock signal to the variety of switches it must control. The dv/dt of a signal thus coupled is typically increased due to the gain of the circuitry, and thus this limitation distinguishes almost all ordinary CMOS IC processing of charge pump clock signals.

The Examiner justifies his assertion that Tasdighi in combination with Yamauchi renders Claim 3 obvious in the following assertion (Office Action mailed December 12, 2007, p. 30 last full sentence, emphasis added):

> Deeming the line coupling the clock output from charge pump clock generating circuit (24 of Tasdighi; Fig. 7 of Yamauchi) to the control nodes of transistors 26,27 as coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of [*sic*] voltage rise or fall, thus rendering claims 3-4 obvious.

The Examiner thus "deems" the arrow to represent circuitry whereby the signal will be coupled to each coupling switch without increasing the rate of rise or fall of the voltage. This assertion is contrary to the overwhelming practice in IC charge pumps. Moreover, it is a further example of this Examiner attributing specific disclosure to references in spite of the plain absence of any such disclosure. The Appellants protest this as a further example of the error described in the remarks of subsection *VII.A.4.d Attributing to References Features That Are Clearly Absent*, which remarks are incorporated here by reference.

Contrary to the Examiner's unsupported assertion, neither Tasdighi nor Yamauchi discloses any such detail as required by Claim 3. An arrow (or line), which is not even intended to be a schematic or other representation of specific components, simply cannot and does not convey the

features required by Claim 3, which, as set forth above, are at least unusual in charge pump designs, and are important aids in achieving noise reduction in charge pumps.

The remarks set forth above support a conclusion that Claim 3 is nonobvious over Tasdighi in view of Yamauchi. Claims 4 and 48 recite limitations generally similar to those remarked on above with respect to Claim 3, which remarks therefore apply *mutatis mutandis* to demonstrate that claims 4 and 48 are also nonobvious over Tasdighi in view of Yamauchi irrespective of the nonobviousness of the claims from which they depend. The panel is therefore respectfully requested to reverse the Examiner's rejection of Claims 3-4 and 48 on this ground.

Claim 10 recites in part: "coupling substantial charge into the transfer capacitor via the charge pump clock output." The same lack of coupling detail in both Tasdighi and Yamauchi remarked upon hereinabove in regard to Claim 3 precludes a conclusion that either reference discloses this requirement, which is a particular feature of the coupling between a clock and a transfer capacitor coupling switch (TCCS). The combination of Tasdighi and Yamauchi accordingly fails to disclose all of the limitations of Claim 10, which is therefore nonobvious over those references irrespective of the nonobviousness of any claims from which it depends.

Misinterpretation of the word "via" The Examiner supports his rejection of Claim 10 over Tasdighi and Yamauchi by stating (Office Action of December 12, 2007, sentence bridging pages 30-31): "Since transfer capacitor C1 will be periodically coupled between voltage source Vin and Gnd in response to the charge pump clock output in order to charge, a substantial charge will be coupled into transfer capacitor C1 during those periods, rendering claim 10 obvious." The Examiner has apparently incorrectly construed the language of Claim 10, which recites (underlining added for emphasis): "coupling substantial charge into the transfer capacitor <u>via</u> the charge pump clock output." The language plainly means that the substantial charge passes through the clock output itself, and <u>not</u>, as the Examiner would have it, that charge is coupled into the transfer capacitor <u>under control of</u> the clock output. The plain meaning of the term "via" is "by way of," not "under control of." This appears to be the Examiner's mistake, because otherwise his rejection is illogical in view of the insulating nature of CMOS gates. Even assuming *arguendo* that the charge pump clock is directly coupled to the gates of the CMOS FETs in SW1 and SW2 (as asserted by the Examiner),

such coupling would clearly not transfer substantial current into C1 "via the charge pump clock output", as set forth in Claim 10. The only current that would be coupled from the clock into C1 in such a charge pump would be tiny amounts due to parasitic gate capacitance of the FETs. The modifier "substantial" is included in Claim 10 precisely to preclude such incidental parasitic charge transfer from "reading on" the claimed limitation. Dictionary definitions of "via" supporting the foregoing remarks are set forth in subsection *VII.B.6.b Rejection of Claim 10 over Forbes in view of Ito*, and are incorporated here by reference.

Because Claim 10 is nonobvious over Tasdighi in view of Yamauchi irrespective of the nonobviousness of the claims from which it depends for the additional reasons set forth above, the panel is respectfully requested to reverse the Examiner's rejection of Claim 10 on this ground.

VII.B.7.c Rejection of Claims 12, 14 and 16 over Tasdighi in view of Yamauchi

A sine-like charge pump clock waveform is contrary to the goals and practices of prior art charge pumps.

The evidence of record supports a conclusion that no charge pump designer in over thirty years of prior art development, despite a number of attempts to address the problem of noise generated by charge pumps, had made the Appellants' fundamental discovery that the clock was an important source of such noise, nor concluded that slowing the clock edges could reduce the noise. Nor had any skilled designer suggested a slow-edged clock waveform, let alone a substantially sine-like waveform. Thus, a sine-like charge pump clock waveform is clearly contrary to the practice of prior art charge pumps.

This aspect of the Appellants' invention is perhaps closest to their fundamental recognition of the problem of noise caused by an overly fast-edged clock. As support for this assertion, the remarks set forth or incorporated by reference in subsections *VII.A.1.d*, *VII.A.1.e*, *VII.A.1.f*, *VII.A.1.g*, and *VII.A.1.h A Fundamental Discovery, Ignored* are incorporated here by reference, as are the remarks set forth in subsections *VII.A.3.a Integrated Circuit Charge Pump Clock Waveforms* and *VII.A.3.b Coupling IC Charge Pump Clock to TC Coupling Switches.*

The numerous examples of charge pump clock waveforms in the prior art of record demonstrate that the waveform desired is a "pulse" or "square" wave. Some references, such as Hara, permitted the clock to become somewhat trapezoidal, yet Hara implied that the clock should not be slowed too much by asserting that ring oscillators for charge pumps should have five or more inverter sections. The proportion of voltage transition time in the output of a ring oscillator, especially a current starved ring oscillator (CSRO), *increases* as the number of inverter stages *decreases*, and increases from about 47% of the waveform to about 70% of the waveform for a CSRO of five stages versus a CSRO of three stages, as described in more detail in the remarks set forth under subheading *A 3-Stage Current Starved Ring Oscillator Generates Undesirably Slow Output Waveform* in subsection *VII.B.2.b Not Obvious to Modify a Charge Pump To Follow Non-Charge Pump Art Ito*, which are incorporated here by reference. Thus, Hara implies that a sine-like clock waveform is contrary to the goals of charge pump prior art.

Further support for the contention that a sine-like clock waveform is contrary to the goals of charge pump prior art is set forth in subsections *VII.A.3.a Integrated Circuit Charge Pump Clock Waveforms* and *VII.A.3.b Coupling IC Charge Pump Clock to TC Coupling Switches*, incorporated by reference above, which support a conclusion that the facility with which ICs manage digital data, compared to analog information, provides strong market motivations to employ fast edged clocks suitable for coupling by active circuitry.

Finally, the principle of *res ipsa loquitur*, combined with the absence of any example of a remotely sine-like clock waveform in the very extensive prior art of charge pumps developed over a span of more than thirty years strongly supports a conclusion that sine-like clock waveforms were considered inimical to IC charge pump design by the brightest and most inventive charge pump designers.

Claim 12 recites in part (underlining added for emphasis):

> c) a charge pump clock generating circuit including an active driver circuit configured to both source current to and sink current from the charge pump clock output to cause a voltage waveform of the charge pump clock output to be substantially sine-like due to
>
> i) circuitry configured to limit source current provided by the active driver circuit to the charge pump clock output, and

ii) circuitry configured to limit current sunk from the charge pump clock output by the active driver circuit.

Tasdighi refers to the clock waveform as a "train of pulses" (col. 3 lines 16-17). This language is consistent with a description of square or rectangular waveforms, and is inconsistent with a description of a sine or sine-like waveform. Yamauchi repeatedly and exclusively describes the oscillator output as a "pulse voltage" (Abstract, four places; throughout the claims; col. 3 lines 51-61 five places; col. 9 line 65 - col. 10 line 13 three places). Thus, the evidence in both cited references is that the clock waveforms are pulses, or a train of pulses. This is entirely consonant with the other prior art of record, which illustrates no clock waveforms that are not rectangular or nearly rectangular

To support the rejection of Claim 12 over Tasdighi in view of Yamauchi, the Examiner states in regard to Yamauchi's Fig. 7 (Office Action of December 12, 2007, page 31 lines 11-12): "The periodic switching of 43 and 45 will effectively provide a CLK waveform that is substantially sine-like." The Examiner points to no evidence in support of this conclusory assertion, nor to any reasoning that might lead to it.

However, the Examiner states in his rejection of Claim 12 as indefinite that he considers any oscillating waveform that is not exactly a square wave to be "substantially sine-like." Subsection *VII.C.1 Meaning of phrase "Substantially Sine-like"* sets forth the Examiner's statement, and sets forth remarks supporting a vastly narrower meaning for the phrase than the Examiner suggests. The remarks of that section are incorporated here by reference. As demonstrated in those remarks, the plain meaning of "substantially sine-like" is a waveform that looks significantly like a sine wave. This plain meaning leads ineluctably to a more detailed description of the required waveform as having quarter cycles that are significantly symmetric to each other, half cycles that are significantly symmetric to each other, no substantial straight-line segments, and no significant sharp angles. Such waveform would be readily recognized by one of skill in the art as looking significantly like a sine wave.

There is no suggestion of such a waveform for an IC charge pump clock output anywhere in the substantial prior art that is of record, and, so far as is known, no such suggestion anywhere in the

prior art of IC charge pumps. Moreover, the prior art is not at all close. The evidence of record indicates that the prior art of IC charge pumps fails to illustrate or suggest a clock output waveform that is even remotely like a sine wave. Thus, not only do Tasdighi and Yamauchi fail to suggest any IC charge pump clock output waveform that is remotely like a sine wave, but one cannot reasonably infer such a waveform, in light of the fact that the entire prior art of IC charge pumps appears to be devoid of such clock output waveforms.

Because neither Tasdighi nor Yamauchi even remotely suggests a substantially sine-like clock output waveform, which would be highly contrary to all the prior art of IC charge pumps, Claim 12 is clearly nonobvious over this combination of references. For purposes of this rejection only, Claims 14 and 16 may stand or fall with Claim 12, from which they properly depend. Accordingly, the panel is respectfully requested to reverse the Examiner's rejection of Claims 12, 14 and 16 on this ground.

VII.B.7.d Rejection of Claims 50-51, 53 and 57-58 over Tasdighi in view of Yamauchi

The Examiner does not assert that Claim 49 is obvious over Tasdighi in view of Yamauchi, but by maintaining rejection of Claims 50-51 and 53 on that ground, he implies that Claim 49, from which those claims properly depend, is also obvious. The nonobviousness of Claims 50-51 and 53 will be therefore be demonstrated by remarks in respect of Claim 49, the subject matter of which is common to all three.

Claim 49 is set forth below (underlining added for emphasis):

> A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:
>
> a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and
>
> b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

Because the Examiner does not assert that Claim 49 is obvious over a combination of Tasdighi and Yamauchi, he provides no statement explaining such rejection. However, it is respectfully submitted that Tasdighi and Yamauchi both fail to disclose, teach or fairly suggest all of the features of Claim 49, particularly those underlined above.

The underlined features of Claim 49 are all details of coupling circuitry between a clock and TCCSs. Remarks set forth, or incorporated by reference, in subsection *VII.B.7.b Rejection of Claims 3-4, 10 and 48 over Tasdighi in view of Yamauchi* are incorporated here by reference to support the Appellants contention that neither reference shows any details of coupling circuitry, and also to register objection to the Examiner's repeated attribution of disclosure to a reference like Tasdighi when such disclosure is plainly absent.

The Examiner has previously asserted that Tasdighi discloses the requirements set forth in Claim 49, and does so by implication in the present rejection. However, Tasdighi discloses neither a single phase clock, nor passive coupling. The required combination of single phase clock and passive coupling to control nodes of the TCCSs, as required in Claim 49, is not disclosed in any prior art of record, and thus the Examiner's attribution of it to the absence of detail in Tasdighi is particularly improper.

The Appellants have previously explained to the Examiner that the circuit he imagines Tasdighi might be suggesting does not work properly, because it would cause at least some concurrent (or "simultaneous") conduction of two TCCSs disposed in series across either a supply, or across the TC, in either event causing current spikes, inefficiency and possibly damage (see, *e.g.*, Amendment After Final Rejection submitted October 11, 2005, last paragraph of page 23 through first paragraph of page 25).

Moreover, there is clear evidence that the circuits that actually underlie the disclosure of Tasdighi use plural clocks, contrary to the requirements of Claim 49. Although Tasdighi does not disclose coupling details, Tasdighi Figure 4 is stated to be the circuit of U.S. Patent 4,897,774 ("Bingham"), which has been made of record. The circuitry of Figure 4 is disclosed in Tasdighi in a representation that is essentially identical to each other switching arrangement, such as Figures 1 and 7. However, Bingham actually contains details illustrating the missing coupling circuitry of Figure

4. Figure 1A of Bingham is identical to Figure 4 of Tasdighi, but Figure 1B illustrates details showing that the TCCSs for each TC of Figure 4 (1A) are controlled by two inverted clock phases. The Examiner's conjecture about the details of coupling that Tasdighi fails to show is improper as a basis for rejecting claims limited by such details, as a matter of basic examination principle; but moreover, the disclosure of Bingham almost conclusively proves that the Examiner's conjecture is not only improper, but simply, completely, wrong.

Yamauchi provides no more disclosure of coupling between the clock and the TCCSs than does Tasdighi, in fact showing only an arrow pointing from "CLK" to "Pump Circuit" 37 (Yamauchi, Figure 5). Thus, both references entirely fail to disclose very significant and otherwise nonobvious requirements set forth in Claim 49, and accordingly fail to support *prima facie* obviousness of Claim 49. Claim 49 is therefore nonobvious over Tasdighi in view of Yamauchi.

Claims 50-51, 53 and 57-58 are nonobvious over Tasdighi in combination with Yamauchi by virtue of depending on Claim 49, for the reasons set forth above. For purposes of this ground of rejection only, Claims 57-58 may stand or fall according to the nonobviousness of Claim 49. Moreover, Claims 50 and 53 each include separate, additional coupling details that are not shown by either Tasdighi or Yamauchi, and are each further nonobvious by virtue of such further coupling requirements. Claim 51 effectively includes the additional limitations set forth in both Claims 50 and 53, and thus is even further distinguished over Tasdighi in view of Yamauchi. Because each of Claims 50-51 and 53 are nonobvious over Tasdighi in view of Yamauchi due to a multiplicity of failures of disclosure in both Tasdighi and Yamauchi, the panel is respectfully requested to reverse the Examiner's rejection of Claims 50-51, 53 and 57-58 on this ground.

VII.B.8 Rejection of Claims 50-51 and 53 over Imamiya, Ito, Yamashiro and Clark

On page 34 of the Office Action issued December 12, 2007, the Examiner rejects Claims 50-51 and 53 as obvious over Imamiya in view of Ito, Yamashiro and Clark. The Examiner does not assert that Claim 49 is obvious over Imamiya, Ito, Yamashiro and Clark, but by maintaining rejection of Claims 50-51 and 53 on that ground, he implies that Claim 49, from which those claims properly depend, is also obvious over that combination. The nonobviousness of Claims 50-51 and

53 will be therefore be demonstrated in part by remarks in respect of Claim 49, the subject matter of which is common to all three.

The remarks set forth or incorporated by reference in subsection *VII.B.1.b Rejection of Claim 49 over Imamiya in view of Pfiffner*, as well as those set forth or incorporated by reference in subsection *VII.B.3.d Rejection of Independent Claim 49 over Imamiya in view of Ito and Yamashiro*, are incorporated here by reference. Those remarks amply support a conclusion that Claim 49 is nonobvious over Imamiya, even in combination with Ito, Yamashiro and or Pfiffner. The failure of the Examiner's asserted rationale for rejecting Claim 49 over Imamiya (whether in combination with non-charge pump art, or not) is that it relies upon disclosure illustrated in Figure 15A. Figure 15A illustrates a "potential converter" as it is called by Imamiya. The potential converter is not a charge pump, which Imamiya describes elsewhere, and does not disclose either a charge pump or a circuit having an output supply, both of which are basic requirements of Claim 49.

As noted in the remarks incorporated by reference above, Imamiya fails to disclose the elements required by Claim 49, even looking to the actual charge pumps that are disclosed in Imamiya (Figures 5 and 10). The most relevant charge pump of Imamiya, illustrated in Figure 10, fails to disclose coupling the clock to a control node of the TC discharging switch. Because this is a detail relevant only to charge pumps, no art that is not directed to charge pumps will include any relevant subject matter that could remedy this failure of Imamiya. Thus, it does not matter whether Ito, Yamashiro, or Pfiffner, or all three, are combined with Imamiya, because the combination cannot and does not disclose all of the important requirements of Claim 49.

For his reasoning in respect of Clark, the Examiner refers to "Applying the same type of reasoning as previously described above with respect to the rejections of claims 50-51 and 53 using only the Imamiya, Ito, and Clark references ..." However, no such rejection is set forth in the Office Action. It is reasonably presumed, however, that the Examiner intends to reference the arguments he set forth in respect of Clark in supporting his rejection of Claims 50-51 and 53 over Imamiya, Pfiffner and Clark.

The Examiner cites Clark exclusively for its disclosure of switches in a flying capacitor type circuit (Office Action issued December 12, 2007, beginning p. 19 line 18, especially p. 20 lines 2-8),

wherein the switches are comprised of two series-connected FETs. That disclosure is relevant to Claims 50-51 and 53, but has no bearing on the requirements of Claim 49. However, as neither Ito nor Yamashiro includes any relevant disclosure to remedy the failure of Imamiya to suggest the features required by Claim 49, Clark is considered for such remedy.

Clark discloses a circuit that is much like the circuit illustrated in Figure 15A of Imamiya. It generates a control signal for a device (*e.g.*, 20a in Figures 1, 2), which is not an output supply but a switch control voltage. There is an intermediate control voltage provided to the "top" of drive circuit 24 from circuit 20, but, as may be seen in both Figures 1 and 2, this is also not a "supply." Having no capacitive storage, such intermediate control voltage will be present, at most, only if switch 40 is closed.

It might be possible that the circuit underlying Clark is relevant to the subject matter that Imamiya fails to teach, though there is no reason to assume so. In any event, Clark does not disclose a clock such as required by Claim 49, and moreover provides no information about coupling any drive source, whether clock or not, to the switches that couple the "fly capacitor" (30 in Figures 1, 2). As such, Clark fails to disclose any subject matter that could possibly remedy the failure of Imamiya to disclose coupling as required by Claim 49.

Ito, Yamashiro and Clark thus have no disclosure that could possibly remedy the failure of Imamiya to suggest all the important elements of Claim 49. The combination of all those references accordingly fails to establish *prima facie* obviousness of Claim 49, which is therefore nonobvious over the combination. For purposes only of this ground of rejection, Claims 50-51 and 53 may rely on the nonobviousness of Claim 49 from which they properly depend. In view of the foregoing remarks, and those incorporated by reference, the panel is therefore respectfully requested to reverse the Examiner's rejection of Claims 50-51 and 53 on this ground.

VII.B.9 Rejection as Obvious over Tasdighi in view of Yamauchi and Pfiffner

On page 33 of the Final Rejection dated December 12, 2007, the Examiner rejects Claim 49 as obvious under 35 USC § 103(a) over Tasdighi in view of Yamauchi, and further in view of Pfiffner.

This ground of rejection is another example of the Examiner's insistence on attributing disclosure to references that are clearly devoid of any such disclosure, without a reasonable basis such as inherency. This systematic examination error by the Examiner is remarked upon hereinabove in subsection *VII.A.4.d Attributing to References Features That Are Clearly Absent* within subsection *VII.A.4 Examination Errors Systematically Repeated by Examiner.*

Claim 49 is set forth below (underlining added for emphasis):

> A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:
> a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and
> b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

As can readily be seen Claim 49 requires very specific features in respect of the coupling between a charge pump clock and the switches (TC charging and discharging switches, or more generally TCCSs) that are under control of the clock. Neither Tasdighi nor Yamauchi disclose any features comparable to those required by elements (a) and (b), and thus the combination of references utterly fails to support *prima facie* obviousness of Claim 49. The contrary contentions of the Examiner are set forth and analyzed below.

The examiner explains this ground of rejection as follows (Office Action of December 12, 2007, p. 33 beginning line 9, underlining added for emphasis and bracketed numerals for reference):

> Related to various rejections previously described above, one of ordinary skill in the art would understand that TC C1 would be coupled to output supply Vout during discharge periods via a TC discharging switch ([1] e.g. 26 will conduct when clock output CLK/Ø is high); and coupling TC C1 to voltage source Vin via a TC charging switch ([1] e.g. 27 will conduct when clock output CLK/Ø is low) during charge periods that nonoverlappingly alternate with the discharge periods. [2] Each of the switches is under control of single-phase charge pump clock output CLK/Ø. It would have been obvious to one of ordinary skill in the art that [3] single-phase charge pump clock output CLK/Ø [4] is passively coupled (e.g. coupled by an [5] interconnecting line with no intervening elements) to the control nodes of the

> charging/discharging switches ([6] e.g. see Tasdighi's transistors 26,27 shown in Fig. 3, with respect to SW1,SW2 shown in Fig. 2), and the gate of each MOS transistor will substantially isolate transfer capacitor (TC) C1 of Tasdighi from Yamauchi's clock output CLK. Therefore, claim 49 is rendered obvious. For example, Pfiffner discloses that "passive elements are ... interconnect lines" on column 1, lines 44-45. Therefore, one of ordinary skill in the art would understand passive coupling does not require any distinct capacitor, resistor, or inductor type elements.

This rationale for rejecting a claim has numerous egregious conjectures, unwarranted assumptions, and misunderstandings of fundamental schematic circuit representations. They are addressed below in turn.

At references [1], the Examiner assumes that CLK/Ø is coupled directly to the "Control" input of FETs 26, 27. This may be accepted only as to ONE Figure 3 circuit. At reference [2], it is indeed reasonable for a pair of switches 26, 27 to be controlled by direct coupling to a single phase of a clock, which may be called CLK/Ø. The assertions to this point are consistent with the prior art, so the fact that they are not actually shown in Tasdighi is not terribly material.

The Examiner further asserts that "it would be obvious" that [3] a single-phase CLK/Ø is passively coupled [4], not to a single switch pair as shown in Figure 3, but to the control inputs of two instances of the Figure 3 circuit, connected to effect the switches SW1 and SW2 [6]. At this point the Examiner is not merely asserting reasonable material that is probably true, even if not actually shown, but has begun wild conjecture that is not only unsupported, but is almost certainly false.

It should not be the Appellants' burden to prove that a reference does not disclose material that it clearly does not show. It should be the Examiner's burden to explain why such material can reasonably be assumed to be present, even if not clearly shown. The Examiner, however, says merely "it would be obvious," without reference or explanation that the Appellants can address. This is an egregious error of examination.

There is a reason that the Examiner insists on relying upon the absence of information in Tasdighi as "rendering obvious" the specific features claimed by the Appellants, and it is this: he cannot find a reference, in all the hundreds that are available, that shows what he wishes to show. In view of that fact, it is inexcusable for the Examiner to blithely assert that such feature is "obvious."

In fact, the Examiner has finally found a reference, Imamiya, which appears to couple a single phase clock passively to TCCS control nodes. As might be expected, the detail in Imamiya shows that the reference fails to comport with Claim 49 for other reasons, as set forth in subsection *VII.B.1.b Rejection of Claim 49 over Imamiya in view of Pfiffner*. Unexpectedly, the Examiner refuses to issue rejections that rely on the charge pumps disclosed in Imamiya, and insists instead on basing his rejections over that reference on "potential converters" shown in Figures 15A,B, but that is a different matter. The Appellants have done their best to address the actual content of Imamiya, rather than that pointed to by the Examiner.

The fact that none of the volumes of prior art that he has searched have disclosed or *reasonably suggested* the features required by Claim 49 should constitute an especially compelling reason for the Examiner to avoid attributing such features to a reference that clearly does not show them. The Examiner, clearly, does not find that reason sufficiently compelling, because he has repeated variations of this rejection for several years, despite persistent objections by the Appellants.

Reference [5] in the inset above of the Examiner's reasoning illustrates either a lack of knowledge or a willful ignorance of such knowledge by the examiner. The "interconnecting line with no intervening elements" to which he refers is, in Figures 2, 8 and somewhat similarly in Figure 7, a line from an oscillator block 24 that points to a block containing switches that are represented by mechanical switch symbols. It is not uncommon that switches, such as SW1,2, are represented by mechanical switch symbols, but it is an indication that they are not to be interpreted literally. The arrow from oscillator 14 or 24 to a switch block is even less literal. It is an arrow, nothing more, and conveys absolutely no electrical detail. (Similarly for Figure 7.)

The Examiner should ask himself how such coupling would actually be achieved, but he has preferred to rely on his bald conjecture, unsupported by any evidence. The Appellants have therefore endeavored to demonstrate to the Examiner that the circuit he asserts "would be obvious" would not, in fact, work properly. Rather than render this Brief even less brief, the analysis is incorporated by reference (Amendment After Final Rejection submitted October 11, 2005, last paragraph of page 23 through first paragraph of page 25). That analysis demonstrates why all of the switches that control a charge pump cannot be passively controlled by direct connection to a single

phase charge pump without causing simultaneous conduction through switches that are disposed in series across either a supply, or across a transfer capacitor. Either circumstance is at least destructive of performance.

Moreover, the Appellants have pointed out to the Examiner that he can see the actual coupling of circuits such as are hinted at in Tasdighi. Tasdighi identifies (col. 3 lines 45-47) the circuit of Figure 4 as incorporated by reference from US Patent 4,897,774 (Bingham, et al., item 18 in evidence appendix). The material of Bingham, incorporated by reference into Tasdighi, illustrates details of the clock/switch coupling. Bingham shows that two inverted clock phases should be used to control the switches of a charge pump. (Figure 1a, phases 44 and 46 controlling the four switches 14a, 16a, 18a and 20a that switch TC 10, and also controlling the four switches 26a, 28a, 30a and 32a that switch TC 24. Figure 2 illustrates how phases 44 and 46 are developed from a single clock source osc. 56.

The coupling illustrated in Bingham, which is in fact incorporated by reference in Tasdighi, which has no other disclosure in this regard, may be interpreted two ways. Phases 44 and 46 may be considered two clock phases. Alternatively, they may be considered a single clock phase that is actively coupled to the switches via the circuitry of Figure 2. Both cases are contrary to the requirements of pending Claim 49.

Thus, not only has the Examiner ignored the protests of the Appellants, ignored the proffered explanations of the Appellants, ignored the basic rules of examination that require attribution only of material that is actually disclosed or reasonably intrinsic, but he has furthermore ignored the teaching (incorporated by reference) of the very reference, Tasdighi, upon which he bases the rejection. As a result of so many errors, it is not surprising to find that the Examiner has baselessly conjectured and assumed a circuit that not only is not shown, but would not work properly. The Appellants greatly regret that this circumstance has caused considerable impatience by their representative.

Yamauchi is focused exclusively on clock generation, albeit for a charge pump, and discloses no detail whatsoever in respect of coupling a clock to transfer switches. Pfiffner is cited only for a proposition that has never been contested, namely that a direct connection constitutes passive coupling, and also contains no disclosure relevant to coupling a charge pump clock to the transfer

switches. Thus, neither Yamauchi nor Pfiffner can remedy any of the many failures of Tasdighi to demonstrate all of the requirements set forth in Claim 49. As such, this combination of references fails to support *prima facie* obviousness of Claim 49. The panel is therefore respectfully requested to reverse the Examiner's rejection of Claim 49 on this ground. The panel is also respectfully requested to clarify to the Examiner the proper use of prior art to demonstrate that a claimed invention is obvious, so as to reduce frustration by other applicants.

VII.B.10 Supporting Remarks: Analysis of Clock Waveforms in Prior Art of Record

The IC charge pump references of record that are known to provide sufficient information to determine a clock output waveform are listed below, together with a brief description of the output waveform(s) they disclose and where the description is located.

The prior art of record indicates that those of skill in the charge pump art almost invariably used clocks having waveforms that were rectangular or nearly rectangular in shape. Those few that deviated from such standard practice did so only slightly or incidentally. Three permitted somewhat trapezoidal waveforms, one described a highly distorted waveform that is difficult to categorize, and one, while primarily describing square waveforms, also described a wave more or less square but having a "lazy" rising edge, plus a sawtooth waveform. None of the waveforms is even remotely sine-like.

Reference:	Clock Waveform (location of information)
U.S. Patent No. 6,411,531 (Nork, et al.)	Rectangular (Figs. 3B, 6B, 8B)
U.S. Patent No. 6,518,829 (Butler)	Rectangular (Figs. 4, 5, 6)
U.S. Patent No. 5,446,418 (Hara, et al.)	Trapezoidal, sharp (Fig. 16)
U.S. Patent No. 4,621,315 (Vaughn, et al.)	Rectangular (Figs. 2)
U.S. Patent No. 4,703,196 (Arakawa)	Rectangular (Fig. 4)
U.S. Patent No. 4,769,784 (Doluca, et al.)	Rectangular (Fig.4)
U.S. Patent No. 5,068,626 (Takagi, et al.)	Rectangular (Figs. 3, 5A, 5B)
U.S. Patent No. 5,111,375 (Marshall)	Rectangular (Fig. 6)
U.S. Patent No. 5,126,590 (Chern).	Trapezoidal timing diagram (Fig. 3)
U.S. Patent No. 6,130,572 (Ghilardelli, et al.)	Rectangular (Figs. 2, 5)

U.S. Patent No.6,816,000 (Miyamitsu)	Rectangular (Figs. 3, 4, 7, 11)
U.S. Patent No. 6,816,001 (Khouri, et al.)	Rectangular (Fig. 7)
U.S. Patent No. 6,825,730 (Sun)	Rectangular (Fig. 3)
U.S. Patent No.6,831,847 (Perry)	Rectangular (Figs. 6a, 6b, applied 6c, 6d)
U.S. Patent No.3,955,353 (Astle)	Rectangular (Figs. 1, 2)
U.S. Patent No.5,306,954 (Chan, et al.)	Rectangular (Figs.3, 5)
U.S. Patent No. 5,193,198 (Yokouchi)	Rectangular (Fig. 5)
U.S. Patent No. 4,839,787 (Kojima, et al.)	Rectangular (col. 4, lines 8-9)
U.S. Patent No. 6,833,745 (Hausmann, et al.)	Rectangular (Fig. 3)
U.S. Patent No. 5,455,794 (Javanifard, et al.)	Rectangular (Fig. 4)
U.S. Patent No. 5,519,360 (Keeth)	Rectangular (col. 3 lines17-19)
U.S. Patent No. 5,553,021 (Kubono, et al.)	Rectangular (col. 9 lines 65-67)
U.S. Patent No. 5,672,992 (Nadd)	Rectangular (Figs. 2, 5, 12)
U.S. Patent No. 5,677,649 (Martin)	Rectangular (col. 6 lines 35-40)
U.S. Patent No. 5,698,877 (Gonzalez)	Rectangular (col. 4 lines 47-48)
U.S. Patent No. 5,786,617 (Merrill, et al.)	Rectangular (Fig. 5b)
U.S. Patent No. 5,889,428 (Young)	Rectangular (Fig. 5, col. 8 lines 46-51)
U.S. Patent No. 5,212,456 (Kovalcik, et al.)	Rectangular (col. 4 lines 6-10 & 35-36)
U.S. Patent No. 3,942,047 (Buchanan)	Rectangular (Fig. 2)
U.S. Patent No. 3,943,428 (Whidden)	Rectangular (col. 3 lines 23-33)
U.S. Patent No. 3,975,671 (Stoll)	Rectangular (col. 2 lines 5-7)
U.S. Patent No. 4,061,929 (Asano)	Rectangular (Figs. 2, 5, 7)
U.S. Patent No. 4,068,295 (Portmann)	Rectangular (Figs. 2, 3, 5)
U.S. Patent No. 4,106,086 (Holbrook, et al.)	Rectangular (Figs. 2, 4, 6)
U.S. Patent No. 4,186,436 (Ishiwatari)	Rectangular (Figs. 2, 3B, 4B)
U.S. Patent No. 4,485,433 (Topich)	Rectangular (Fig. 2)
U.S. Patent No. 6,717,458 (Potanin, Vladislav)	Rectangular (Figs. 6)
U.S. Patent No. 6,486,729 (Imamiya, Kenichi)	Rectangular (Figs. 6, 17)
U.S. Patent No. 6,429,632 B1 (Forbes et al.)	Trapezoidal, asymmetric (Figs. 10, 11, 13)
U.S. Patent No. 6,195,307 (Umezawa et al.)	Rectangular (Figs. 2, col. 9 lines 7-11)
U.S. Patent No. 6,020,781 (Fujioka, Shiny)	Rectangular (pulses, col.5 lines 20-25)
U.S. Patent No. 5,892,400 (van Saders et al.)	Rectangular (Figs. 4, 6, 8A, 9A)

U.S. Patent No. 5,670,907 (Gorecki et al.)	Rectangular (col. 7 lines 44-45)
U.S. Patent No. 5,208,557 (Kersh, Ill, David)	Asymmetric distorted trapezoidal (Figs 6a, 6b)
U.S. Patent No. 5,182,529 (Chern, Wen-Foo)	Rectangular (col.1 lines 12-14; col.4 lines 58-59)
U.S. Patent No. 4,739,191 (Puar, Deepraj S.)	Rectangular (col. 2 lines 20-30)
U.S. Patent No. 4,390,798 (Kurafuji, Setsuo)	Rectangular (Figs. 2, 7c, 9a);
"	Rectangular, slow rise time (Fig. 4e);
"	Sawtooth (Fig. 5e)
U.S. Patent No. 5,808,505 (Tsukada, Shyuichi)	Rectangular (Figs. col. 3 line 47-col. 4 line 5)
U.S. Patent No. 6,122,185 (Utsunomiya et al)	Rectangular (P1 in Figs. 10,11)
U.S. Patent No. 6,169,444 (Thurber, Jr., Charles)	Rectangular (col. 5 lines 55-57)

50 references are IC charge pumps that have enough information to determine clock waveform. Of these 50, 45 describe only rectangular (or pulse) waveforms. Three illustrations suggest trapezoidal waveforms (Hara, Chern '590, and Forbes). However, the clocks in Chern '590 are the outputs from a series of digital gates, and are thus expected to be very "square;" thus the waveform illustration is believed greatly exaggerated for purposes of illustrating relative timing of the different phases of the clock. Forbes describes the relevant figures as "phase/clock timing diagrams" (Brief Description of the Drawings, col. 4), and they are also believed to be exaggerated for illustration rather than representative of the actual waveform. The waveform of Hara Figure 16 is believed to represent an output of the five-stage conventional (not current starved) ring oscillator of Figure 15. One reference (Kersh) illustrates realistic waveforms that are greatly distorted and highly asymmetrical, especially between quarter cycles. One reference (Kurafuji) illustrates rectangular waveforms in three places, but also illustrates a clock output having a rectangular waveform with a "lazy" leading edge (Fig. 4e), and a sawtooth waveform (Fig. 5e).

The charge pumps of record, insofar as the Appellants' representative can ascertain, contain not the slightest suggestion that even somewhat sine-like waveforms might be even marginally acceptable, let alone substantially sine-like waveforms. Moreover, Hara teaches that current starved ring oscillators should not have less than the five inverter stages. Because fewer stages causes the waveform to be less square (other parameters held constant), and because no prior art waveform is

significantly less square than is shown in Fig. 16 of Hara, the clear implication is that the conventional wisdom teaches away from any remotely sine-like waveform.

VII.C. Rejections Under 35 USC § 112, Second Paragraph

On page 6 of the Final Rejection dated December 12, 2007, the Examiner rejects Claims 1-10, 12-17, 20, 28-41 and 68 under 35 USC § 112, second paragraph, as being indefinite. Claim 62 may also stand thus rejected; the Examiner is not definite in this regard.

Interpretation of the definiteness requirement of 35 USC § 112, second paragraph, has gradually become more tolerant of claim drafting imperfections. The test has long been whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081 (Fed. Cir. 1986). Recent interpretation by the Federal Circuit is even more forgiving: "When a claim is not insolubly ambiguous, it is not invalid for indefiniteness." *Marley Mouldings, Ltd., v. Mikron Indus.*, 417 F.3d 1356, 1361, 75 U.S.P.Q.2D 1954 (Fed. Cir. 2005), citing *Bancorp Servs., L.L.C. v. Hartford Life Ins. Co.*, 359 F.3d 1367, 69 USPQ2d 1996 (Fed .Cir. 2004).

VII.C.1 Meaning of the phrase "Substantially Sine-like"

When "substantially" is used with a precise relationship, the relationship is readily understood. For example, the court in *Andrew Corp. v. Gabriel Electronics,* 847 F.2d 819, 822, 6 USPQ2d 2010 (Fed. Cir. 1988) held that the limitation "which produces substantially equal E and H plane illumination patterns" was definite because one of ordinary skill in the art would know what was meant by "substantially equal." A "sine wave" is a mathematical relationship as precise as the mathematical meaning of "equal." A "substantially sine-like" waveform is not less precise than "substantially equal ... illumination patterns."

The Examiner states (Office Action issued December 12, 2007, page 6 beginning line 19, underlining added for emphasis):

> The phrase "substantially sine-like" in claims 12 (line 9), 20 (line 3), and 28 (line 10) is still considered relative, rendering the claims, and their corresponding dependent claims (if any), indefinite. The phrase is not defined by the claim, the specification does not provide a

> standard for ascertaining the requisite degree, one of ordinary skill in the art would not be reasonably appraised of the scope of the invention, and the applicants' present and previous comments have never clearly described what it actually means. For example, until the applicant clearly defines what is meant by "substantially sine-like", this examiner will still assume that any signal that is neither clearly shown nor described as a true square (or rectangular) wave that has sharp rising and falling edges (e.g. no, or at least minimal, transition times) will be considered "substantially sine-like"? These signals would include those that have at least one rising or falling edge that gradually changes in either a linear or non-linear manner (e.g. the transition between a logic high level and logic low level is not substantially instantaneous).

The Examiner's interpretation is beyond reasonable in view of the plain meaning of "substantially like" and the precise mathematical shape of a sine wave. However, the Examiner's request for clarification is one to which the law permits and even encourages an answer. Relying on such an answer can properly lay to rest all the uncertainty the Examiner expresses as to the scope of the term, while yet providing the Appellants the benefit of their fundamental discovery and invention.

It is a basic tenet of claim construction that a limitation is given its plain meaning, *i.e.*, its ordinary and customary meaning, unless the applicant or patentee has made a contrary meaning clear in the specification. "In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art." *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298, 67 USPQ2d 1132, 1136 (Fed. Cir. 2003). The usual and customary meaning of a term may be evidenced by a variety of sources, such as dictionaries (*Tex. Digital Sys., Inc., v. Telegenix, Inc.*, 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1818 (Fed. Cir. 2002)).

In the present case, the plain, usual and customary meaning of a "sine" waveform is based on a mathematical definition that is fundamental to the education of electrical engineers. A dictionary definition is provided (underlining added): a "sine wave" is defined as "a periodic oscillation, as a sound wave, having the same geometric representation as a sine function." In the same dictionary, a "sine curve" is defined as "a curve described by the equation $y = \sin x$, the ordinate being equal to the sine of the abscissa." ("Webster's Encyclopedic Unabridged Dictionary of the English Language," pub. Gramercy Books, copyright 1989 by dilithium Press, Ltd.).

Construction of the phrase "substantially sine-like" is properly based on the plain and ordinary meaning of its terms, unless the Appellants have expressed a contrary intention (see MPEP 2111.01 and, *e.g.*, *Brookhill-Wilk, id.*). In this regard the Appellants' specification states (page 12 lines 23-26):

> The current starved ring oscillator 500 is also an exemplary circuit for producing a charge pump clock output 524 for which dv/dt is actively limited in both negative and positive transitions. Voltage of the CLK output 524 may oscillate substantially rail-to-rail (*e.g.*, between 0 to Vin+) with low dv/dt transitions, and may have a significantly sine-like shape.

The plain meaning of "a significantly sine-like shape" or "substantially sine-like" is that the waveform is very much like a sine wave, yet is permitted some latitude of deviation from a precise sine wave. A sine wave, of course, is precisely defined mathematically such that it has no breadth at all. But to have a "significantly sine-like shape," or to be "substantially sine-like," both requires and is caused by appearance characteristics that are all significantly like those of all parts of a sine wave. As a first example, a sine wave cycle has four quarter cycles, each occupying a time position corresponding to degrees from zero to 90, 90 to 180, 180 to 270 and 270 to 360 in a generalized sine wave. Each of the four quarter cycles is precisely symmetric with each other quarter cycle. Therefore, a substantially sine-like waveform must have a complete cycle that is comprised of four quarter cycles, each significantly symmetrical with the others. Similarly, a sine wave has two half cycles corresponding to zero to 180 degrees and 180 degrees to 360 degrees, and these are symmetrical about the average voltage. Thus, a substantially sine-like wave cycle must be comprised of two half cycles that are significantly symmetric to each other. A sine wave has no straight-line segments, and thus a substantially sine-like waveform has no significant straight-line segments. A sine wave has no sharp angles at all, and hence a substantially sine-like waveform has no significant sharp angles. All of these things follow ineluctably from the plain meaning of having a shape that is significantly like a sine wave, as set forth in the text. The waveform will of course *look* much like a sine wave, as will readily be seen by persons of skill in the art; the overall required appearance of the waveform, and the more detailed aspects of such appearance follow from each other.

The description of a "substantially sine-like" waveform thus has four substantially symmetrical quarter cycles and two substantially symmetrical half cycles, no significant straight-line segments, and no significant sharp angles. Such a waveform is easy to compare to other waveforms, nearly all of which have significant sharp angles, substantial straight line segments, and/or are significantly asymmetrical. What is more, when the meaning of "substantially sine-like" is thus looked at closely, a "substantially sine-like" output from an IC charge pump clock is readily seen to be vastly different than descriptions of clock output waveforms in the prior art of IC charge pumps.

The phrase "significantly sine-like shape" is very clear to practicing engineers, *i.e.*, persons of ordinary skill in the art of charge pump design, as indicating an oscillating waveform having a shape that is a great deal like a sine wave, which as noted above has a precise mathematical definition. As remarked above, the requirement that the waveform look significantly like a sine wave entails features, such as significant symmetry, no significant straight segments, and no significant sharp angles. Thus, the phrase clearly does not cover waveforms that are less like sine waves than like square waves, trapezoidal waves, sawtooth waves, triangle waves, or any other common waveform. The person of skill in the art will also understand that a waveform need not be a perfect sinusoid to be "substantially sine-like," thus permitting some aberration in an otherwise sine-like shape.

It is important to note that the prior art of charge pumps is not close to disclosing a "substantially sine-like" waveform. Hara, Figure 16, is trapezoidal, as are timing diagrams in Chern '590 and Forbes; one waveform is sawtooth, one is distorted and asymmetrical, one is a square wave with a rounded rising waveform, but the vast majority of the roughly one hundred illustrations or descriptions are of rectangular or pulse waveforms. The remarks set forth in subsection *VII.B.10 Supporting Remarks: Analysis of Clock Waveforms in Prior Art of Record* are incorporated here by reference, elaborating on the waveforms and identifying where they are found in each IC charge pump reference of record that includes such information. None of the waveforms are described or illustrated as remotely close to a sine waveform.

If the prior art were close, it would be proper to require an explanation that would permit a close description of the bounds of the claimed subject matter to ensure that it does not encompass

prior art. In the present circumstances, however, the prior art is not close. There is a huge gap between the claimed "significantly sine-like" clock output, and the closest suggestion in the prior art of IC charge pumps, which shows a steep-edged trapezoidal waveform.

The Federal set forth the following analysis of the law in respect to indefiniteness in Eveready Battery Co. v. International Trade Commission: *EBC v. ITC*, 435 F.3d 1366 (Fed. Cir. 2006)(selected text underlined and boldface for emphasis):

> An analysis of claim indefiniteness under § 112 P2 is "inextricably intertwined with claim construction." *Atmel Corp. v. Information Storage Devices, Inc.*, 198 F.3d 1374, 1379 (Fed. Cir. 1999). See *Datamize v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347-48 (Fed. Cir. 2005) ("'By **finding claims indefinite only if reasonable efforts at claim construction prove futile**, we accord respect to the statutory presumption of validity and **we protect the inventive contribution of patentees, even when the drafting of their patents has been less than ideal**.'") (quoting *Exxon Research & Eng'g Co. v United States*, 265 F.3d 1371, 1375 (Fed Cir 2001)); *Oakley, Inc. v. Sunglass Hut Int'l*, 316 F.3d 1331, 1340-41 (Fed. Cir. 2003) (determination of claim definiteness "requires a construction of the claims according to the familiar canons of claim construction"). Accordingly, we give de novo review to the Commission's ruling of patent invalidity for claim indefiniteness.
>
> 35 U.S.C. § 112 P2 requires that the patent specification shall "conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." This provision both facilitates examination during the patent application stage, and upon grant serves to notify the public of what is patented. The reviewing tribunal must determine whether a person experienced in the field of the invention would understand the scope of the claim when read in light of the specification. See *Howmedica Osteonics Corp. v. Tranquil Prospects, Ltd.*, 401 F.3d 1367, 1371 (Fed. Cir. 2005) (claim not indefinite due to ambiguity when meaning readily ascertained from the description in the specification); *Personalized Media Communs., L.L.C. v. ITC*, 161 F.3d 696, 705 (Fed. Cir. 1998). See generally *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en *banc*) (**claims are construed in the context of the specification and prosecution history, as they would be understood by persons in the same field of endeavor**).

As may be seen, the Federal Circuit is reluctant to hold claims indefinite if they can reasonably be construed. As illustrated by the remarks set forth above, the phrase in question can very reasonably be construed. Further, the court is motivated to "protect the inventive contribution of patentees, even when the drafting of their patents has been less than ideal." In drafting the subject specification, "a significantly sine-like shape" was believed so abundantly clear to those of skill in the art that elaboration was unnecessary. Indeed, as noted above, the plain meaning of the phrase

"substantially sine-like" provides a variety of specific features that follow from the plain meaning of "substantially like a sine wave." In retrospect the application would have more ideally drafted, and would have incurred less opposition from the Examiner, had the phrase "significantly sine-like shape" been substantially elaborated. Nonetheless, the Appellants have made a dramatic discovery of a fundamental nature, which is very surprising because the field of IC charge pumps is quite mature and very crowded. As such, the inventors are properly entitled to protection for their contribution.

Because the proffered analysis of the plain meaning of "substantially sine-like" may properly be relied upon by the panel or the Examiner to find claims setting forth such phrase to be definite, and because the prosecution history itself significantly controls claim construction, there need be no ambiguity in any future claim construction exercise in respect of the term "substantially sine-like."

Despite the brevity of the description in the Appellants' specification, the precision of the mathematical definition of "sine wave," in combination with the many aspects of such waves that must be closely matched to satisfy the description of having a "significantly sine-like shape," provides ample features that serve to easily distinguish the bounds of subject matter encompassed by such phrase. In view of the plain meaning of the terms, and considering that the subject matter covered by "substantially sine-like" differs dramatically from the teaching and disclosure of all IC charge pump prior art, the panel is respectfully requested to hold the phrase definite. By so doing, the panel will protect the highly inventive contribution of the inventors despite less than ideal drafting, and will leave no significant ambiguity as to the meaning of the claim.

VII.C.2 Specific Rejections for Indefiniteness

The Examiner maintains rejections of Claims 1-10, 12-17, 20, 28-41 and 68 under 35 USC § 112, second paragraph, as being indefinite. He rejects Claim 1 for failing to exclude ring oscillators having an odd number of less than three inverter stages, and rejects Claims 2-10 due to incorporating the language of Claim 1 by virtue of depending therefrom. He may be maintaining a rejection of Claim 10 as indefinite for reciting "coupling substantial charge into the transfer capacitor via the charge pump clock input [*sic* output]." He rejects Claims 12, 20 and 28 as indefinite for relative language due to reciting that a waveform is limited to being "substantially sine-like," which rejection

applies as well to Claims 13-17 and 29-41 by virtue of depending from Claims 12 and 28, respectively.

VII.C.2.a Rejection of Claims 1-10 and 68 as Indefinite

The Examiner asserts that Claims 1-10 and 68 are indefinite by virtue of ambiguity in Claim 1. In particular, the Examiner states:

> It is still not understood in claim 1 how an implied single inverting driver section (i.e. an odd number less than three) can be "sequentially cascaded", wherein "cascaded" implies a series of more than one component. Therefore, it is suggested the "sequentially cascaded" phrasing be removed from claim 1 and added to claim 68, which is understood to have three driver sections.

It is a straightforward matter to fabricate an oscillator having a single inverter stage coupled in series with itself. The only issue is definitional, in particular, whether a "ring oscillator" having only a single inverter stage may be "cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section," as required by Claim 1.

If it is possible, as the Appellants believe, then it is simple to fabricate. But if an oscillator consisting of a single inverter stage coupled in series with itself is deemed not to be a "ring oscillator," or not to satisfy the requirement of being "cascaded sequentially in a ring," then by its terms Claim 1 simply does not apply to such an oscillator. Claim 1 would still cover a ring of three inverter stages, because the phrase "an odd number of not more than three" covers "three" stages, whether or not it can cover "one" stage. The meaning of the phrase, if it cannot mean one, is simply "three." If it cannot be less than three, then "not more than" is harmless superfluous language.

However, the Appellants are not presently convinced that a single-stage ring oscillator is necessarily an impossibility, or a contradiction in terms. The Appellants considered from the earliest drafting of the subject application that comprising "not more than three inverter stages" is an important requirement for the current starved ring oscillator, because the goal is to generate a clock that is sufficiently slow, or even sine-like. A single current starved inverter stage ring oscillator would tend to be very slow edged compared to its period, or to have a large proportion of transition

time, and thus might be perfectly suitable to achieve the goal of creating a "slow" clock waveform, with its unexpected benefit of generating low noise.

Thus, if a single stage ring oscillator is a ring oscillator and satisfies the other requirements of Claim 1, then such oscillator is covered by Claim 1. That protects the inventors from having their claims avoided by the simple expedient of reducing the number of inverters from three to one. If, on the other hand, such an oscillator is not a ring oscillator (and if it cannot be, then it certainly is not) or such a configuration does not satisfy the other requirements of Claim 1 (and if it cannot satisfy such requirements, then it certainly does not), then such configuration is simply not covered by the terms of Claim 1.

To leave open to the inventors the possibility, to be settled someday perhaps by expert opinion, that a single inverter stage "ring oscillator" is possible without undue experimentation, the Examiner need only tolerate three words "not more than," which he considers at best extraneous. However, the words in no way detract from coverage of an embodiment having three inverter stages in a ring, and as such are harmless.

In response to the Examiner's suggestion that "sequentially cascaded" be deleted from Claim 1, the Appellants observe that such removal would potentially cause Claim 1 not to properly cover a current starved ring oscillator embodiment having three inverter stages.

The panel is therefore respectfully requested to set aside a question, which it need not answer, as to whether a single inverter stage coupled in series with itself satisfies the requirements set forth in Claim 1. If it does not, there is no harm, and if it does then such embodiment is properly covered by the terms.

The MPEP addresses an issue of whether a claim encompassing a non-operative embodiment is indefinite. The guidance of this section is helpful if Claim 1 is deemed to "cover" an embodiment of one stage, but such embodiment is deemed inoperative. One way of looking at a circumstance in which a single inverter stage ring oscillator is not possible is, of course, to deem the embodiment "covered" but "inoperative." MPEP § 2164.08(b) "Inoperative Subject Matter" states:

> The presence of inoperative embodiments within the scope of a claim does not necessarily render a claim nonenabled. The standard is whether a skilled person could determine which

> embodiments that were conceived, but not yet made, would be inoperative or operative with expenditure of no more effort than is normally required in the art. *Atlas Powder Co. v. E.I. du Pont de Nemours & Co.*, 750 F.2d 1569, 1577, 224 USPQ 409, 414 (Fed. Cir. 1984) (prophetic examples do not make the disclosure nonenabling).

The remarks set forth above support a conclusion that the drafting of Claim 1 so as to cover two types of embodiments, one of which might possibly be deemed impossible or not in conformance with the remainder of Claim 1, does not render the claim indefinite, or not enabled, or otherwise in conflict with the requirements of 35 USC § 112. As such, the panel is respectfully requested to reverse the Examiner's rejection of Claim 1 as indefinite on this ground, thereby also remedying the rejection of Claims 2-9 and 68. As the Examiner appears to reject Claims 2-9 and 68 as indefinite only by virtue of depending from Claim 1, those claims will no longer stand rejected on this ground after reversal of the rejection of Claim 1 on this ground.

VII.C.2.b Rejection of Claim 10 as Indefinite

The Examiner appears to reject Claim 10 as indefinite due to a limitation requiring "coupling substantial charge into the transfer capacitor via the charge pump clock output." In particular, he questions which TCCS(s) are controlled to couple the TC to a voltage source as required by Claim 10 by virtue of depending from Claim 1?

The control exerted over TCCSs by the clock in Claim 1 is not limited to direct control by coupling to a control node of a TCCS, but may include indirect control to switches that turn on or off according the voltages across them that are caused by the clock. Thus, during the charging periods, the TC 702 is coupled to a voltage source (common and Vdd, not shown) via the TCCS 704, which is turned on under control of the clock when it reaches a sufficiently high voltage to forward bias the diode-connected FET 704. (During the charging period it is also coupled to the supply Vdd/ground via the clock itself, but that is not a TCCS.) During the discharge periods TC 702 is coupled to the output via TCCS 706 when the clock causes the voltage between 704 and 706 to drop sufficiently low to turn on diode-connected FET 706. It is clear that substantial ... indeed all ... charge is coupled into TC 702 via the output of the clock 524.

Figure 7 illustrates the class or type of charge pump designated "direct TC drive" herein, to distinguish that type from "control only" charge pumps that do not provide substantial charge to the TC via the clock output, as is required by Claim 10. (Relevant remarks set forth or incorporated by reference in subsection *V.D.1 Two Types of Charge Pumps* fully explain these two types of charge pumps and are incorporated by reference for that purpose.) Thus, Claim 10 does not cover "control only" charge pumps.

The panel is respectfully requested to reverse any rejection the Examiner may be maintaining of Claim 10 as indefinite, in view of the fact that the claim terms are clear and reasonably precise.

VII.C.2.c Rejection of Claims 12-17, 20 and 29-41 as Indefinite

Claims 12, 20 and 28 each include the phrase "substantially sine-like" in regard to an IC charge pump clock output waveform. By the plain meaning of its terms, particularly in view of the specification statement that the waveform "may have a significantly sine-like shape," this phrase can only cover waveforms that have a repetitive cycle including four quarter cycles that are all significantly symmetrical with each other, as well as two half cycles that are significantly symmetrical with each other, that have no significant straight line segments, and have no significant sharp angles. Such a waveform will appear much like a sine wave to a person of ordinary skill in the art, who will readily recognize that no prior art of record discloses a clock output waveform for a charge pump that is close to this requirement.

The remarks set forth in subsection *VII.C.1 Meaning of the phrase "Substantially Sine-like"* support the above statements. Those incorporated remarks support a conclusion that due to the plain meaning of the terms, in combination with considerations of reasonable claim construction and fairness to the inventors, the panel should properly deem the phrase definite, and thereby dispel the ambiguity that the Examiner contends is a result of the phrase.

Accordingly, the panel is respectfully requested to conclude that the plain meaning of "substantially sine-like" is definite, and to therefore reverse the Examiners rejection of Claims 12, 20 and 28 as indefinite.

VII.C.2.d Rejection of Claim 62 as Indefinite

The Examiner states: "It is not clear what ""an average voltage"" relates to on lines 2-3 of Claim 62 (Office Action of December 12, 2007, page 7 lines 8-9). Because this is in the section listed as rejections under 35 USC 112, the Examiner appears to be rejecting Claim 62 on this ground.

Claim 62 recites (underlining added for emphasis):

> The method of Claim 61, further comprising biasing each of the capacitive coupling networks such that the TC charging or discharging switch to which it is coupled is nonconductive when the charge pump clock output is at an average value of its time-varying voltage.

The third underlined portion indicates that "an average voltage" relates to the time-varying voltage of the charge pump clock output. That output will have a voltage that will change across time. Because the output is from an oscillator typically producing a slow or even sine-like waveform, the meaning may be considered by imagining that the output is a sine wave. A sine wave need not be centered on zero volts, but may be offset by some amount. For example, a sine wave might extend from 0.2V minimum to 2.2V maximum. In that case, the average voltage of the waveform would be 1.2 V, as may be deduced because of the well known symmetry of a sine wave.

The waveform need not be a sine wave, but in any event it will have a maximum and a minimum. "An average value" of a waveform technically means the average over all time of each instantaneous voltage of the waveform. As a practical matter it is typically measured over just one normal cycle. For many waveforms, especially those that have symmetrical half cycles, the average value will simply be the point midway between the voltage extremes. The average value can be measured for any repetitive waveform.

The reason that this matters is that if the biasing is established as required, then all TCCSs controlled by such clock will be off at the same instant, when the clock waveform travels through its average value.

This claim seems entirely clear and definite, and the panel is accordingly respectfully requested to reverse any rejection the Examiner may be maintaining of Claim 62 as indefinite.

Conclusion

The evidence, law and arguments set forth above address every ground of rejection under 35 USC 102 or 103. Law and arguments are also set forth above that support a conclusion that the Examiner should be reversed as to most of the rejections under 35 USC 112, second paragraph, and such reversal as to each ground of objection thus addressed is respectfully requested.

It is again respectfully submitted that the proffered Amendment After Final Rejection should be entered as placing all claims of the application into condition for allowance.

The Commissioner is requested to construe this Appeal Brief as including a petition to extend the period for submission under 37 CFR 1.136(a) by the number of months necessary to make this submission timely filed. Fees or deficiencies required to cause this Appeal Brief to be complete and timely filed may be charged, and any overpayments should be credited, to our Deposit Account No. **50-0490**.

Respectfully submitted,

12/9/2008
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VIII. CLAIMS APPENDIX

1. Charge pump apparatus for generating an output voltage supply within a circuit, comprising:

a) a transfer capacitor;

b) a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output; and

c) a charge pump clock generating circuit including a ring oscillator comprising an odd number of not more than three inverting driver sections cascaded sequentially in a ring such that each driver section has an output coupled to a next driver section input, wherein a first driver section is next after a last driver section and one of the driver section outputs constitutes a particular charge pump clock output controlling at least one of the transfer capacitor coupling switches, and wherein each driver section includes

i) circuitry configured as an active current limit to limit a rate of rise of voltage at the driver section output, and

ii) circuitry configured as an active current limit to limit a rate of fall of voltage at the driver section output;

d) wherein the plurality of transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times.

2. The apparatus of Claim 68, wherein the plurality of transfer capacitor coupling switches are under control of the particular charge pump clock output.

3. The apparatus of Claim 2, further comprising coupling circuitry configured to couple the particular charge pump clock output as a signal to each of the transfer capacitor coupling switches without increasing a rate of voltage rise or fall of the signal.

4. The apparatus of Claim 68, further comprising a coupling circuit configured to couple the particular charge pump clock output as a signal to the at least one transfer capacitor coupling switch without increasing a rate of voltage rise or fall of the signal.

5. The apparatus of Claim 68, further comprising a capacitive coupling circuit configured to couple one of the at least one charge pump clock outputs to a control node of one of the plurality of transfer capacitor coupling switches.

6. The apparatus of Claim 2, further comprising corresponding capacitive coupling circuits to couple a control node of each of the plurality of transfer capacitor coupling switches to the particular charge pump clock output.

7. The apparatus of Claim 6, wherein none of the corresponding capacitive coupling circuits is configured to conduct substantial charge to the transfer capacitor.

8. The apparatus of Claim 5, wherein the capacitive coupling circuit does not conduct substantial charge to the transfer capacitor.

9. The apparatus of Claim 68, wherein the active current limit circuitry of (c)(i) and (c)(ii) is further configured to limit source and sink currents, conducted by each driver section within the charge pump clock generating circuit, to substantially identical magnitudes.

10. The apparatus of Claim 68, further comprising coupling substantial charge into the transfer capacitor via the charge pump clock output.

11. Charge pump apparatus for generating an output voltage supply within a circuit, comprising:

a) a transfer capacitor;

b) a plurality of transfer capacitor coupling switches, each switchable between a conducting state and a nonconducting state under control of a charge pump clock output and including

i) a common discharge switch disposed between a terminal of the transfer capacitor and a common reference connection of the output voltage supply, and having a first control node AC impedance, and

ii) an output supply discharge switch disposed between an opposite terminal of the transfer capacitor and a connection of the output voltage supply opposite the common reference connection, and having a second control node AC impedance at least twice the first control node AC impedance; and

c) a charge pump clock generating circuit including

i) circuitry configured to limit a rate of rise of the charge pump clock output, and

ii) circuitry configured to limit a rate of fall of the charge pump clock output;

d) wherein the transfer capacitor coupling switches are coupled to the transfer capacitor, and are controlled so as to couple the transfer capacitor to a voltage source during periodic first times, and to couple the transfer capacitor to the output voltage supply during periodic second times that are not concurrent with the first times.

12. Charge pump apparatus within a monolithic integrated circuit for generating an output voltage supply, comprising:

a) a transfer capacitor coupled alternately between source connections and output connections;

b) a plurality of active switches, each switchable between a conducting state and a nonconducting state under control of at least one charge pump clock output to couple charge, which is not substantially conducted by the charge pump clock output, from the source connections to the output connections;

c) a charge pump clock generating circuit including an active driver circuit configured to both source current to and sink current from the charge pump clock output to cause a voltage waveform of the charge pump clock output to be substantially sine-like due to

i) circuitry configured to limit source current provided by the active driver circuit to the charge pump clock output, and

ii) circuitry configured to limit current sunk from the charge pump clock output by the active driver circuit.

13. The apparatus of Claim 12, wherein the charge pump clock generating circuit c) further comprises a discrete capacitive element coupled to the charge pump clock output and configured to reduce voltage rates of change at the charge pump clock output.

14. The apparatus of Claim 12, wherein the charge pump clock generating circuit includes a plurality of active driver circuits each configured to both source and sink current with respect to a corresponding driver output node, and wherein the charge pump clock generating circuit includes circuitry to limit the current source capacity of each of the active driver circuits and circuitry to limit the current sink capacity of each of the active driver circuits with respect to the corresponding driver output node.

15. The apparatus of Claim 12, further comprising one or more capacitive coupling networks configured to couple one of the at least one charge pump clock outputs to a control node of at least one of the plurality of active switches.

16. The apparatus of Claim 12, wherein the charge pump clock generating circuit is configured as a current starved ring oscillator.

17. The apparatus of Claim 12, wherein the source current circuitry c) i) and the sink current circuitry c) ii) are configured to limit source and sink currents to a substantially identical magnitude.

18. Charge pump apparatus for generating an output voltage supply within a monolithic integrated circuit, comprising:

a) a transfer capacitor;

b) one or more source switching devices disposed in series between the transfer capacitor and a voltage source to convey transfer current to the transfer capacitor from the voltage source when conducting;

c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply to convey transfer current from the transfer capacitor to the output voltage supply when conducting; and

d) a charge pump clock generating circuit configured to provide a single-phase charge pump clock output coupled passively, without conveying substantial transfer current, to control nodes of each of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled passively, without conveying substantial transfer current, to control nodes of each of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices, wherein the charge periods alternate with, and do not overlap, the discharge periods.

19. The apparatus of Claim 18, which includes a first charge pump having at least a first example of each recited feature, further comprising a second charge pump stage including:

e) a second transfer capacitor;

f) one or more second-source switching devices disposed in series between the second transfer capacitor and a second voltage source; and

g) one or more second-output switching devices disposed in series between the second transfer capacitor and a second output voltage supply;

h) wherein the charge pump clock output is coupled to all of the second-source switching devices to cause conduction during the charge periods and nonconduction during the discharge periods, and is

coupled to all of the second-output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods.

20. The apparatus of Claim 18, further comprising circuitry configured to reduce voltage change rates of the charge pump clock output during both positive and negative transitions compared to an absence of such circuitry such that the charge pump clock output voltage is substantially sine-like.

21. Charge pump apparatus for generating an output voltage supply within a circuit, comprising:

a) a transfer capacitor;

b) one or more source switching devices disposed in series between the transfer capacitor and a voltage source;

c) a first output switching device having a first device area disposed between a first terminal of the transfer capacitor and the output voltage supply, and a second output switching device disposed between a common reference connection of the output voltage supply and a second terminal of the transfer capacitor opposite the first terminal of the transfer capacitor, having a second device area that is greater than double the first device area; and

d) a charge pump clock generating circuit configured to provide a single-phase charge pump clock output coupled to all of the source switching devices to cause conduction during charge periods and nonconduction during discharge periods for all of the source switching devices, the charge pump clock output further coupled to all of the output switching devices to cause nonconduction during the charge periods and conduction during the discharge periods for all of the output switching devices.

22. The apparatus of Claim 18, wherein the charge pump clock generating circuit (d) further comprises circuitry configured to limit currents conducted by each amplifying driver circuit in the charge pump clock generating circuit.

23. The apparatus of Claim 22, further comprising a discrete capacitive device coupled to an output of one of the amplifying driver circuits to limit a rate of voltage change of the driver circuit output.

24. Charge pump apparatus for generating an output voltage supply within a monolithic integrated circuit, comprising:

a) a transfer capacitor for conveying charge from a voltage source to the output voltage supply;

b) one or more source switching devices disposed in series between the transfer capacitor and the voltage source, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source;

c) one or more output switching devices disposed in series between the transfer capacitor and the output voltage supply, each having a corresponding control node that is substantially isolated from both the transfer capacitor and the voltage source; and

d) a capacitive coupling circuit coupling a charge pump clock output to one of the control nodes corresponding to a source switching device or to an output switching device.

25. The apparatus of Claim 24, wherein the capacitive coupling circuit is a first capacitive coupling circuit coupling the charge pump clock output to a source switching device control node, and further comprising a second capacitive coupling circuit coupling the charge pump clock output to an output switching device control node.

26. The apparatus of Claim 25, wherein each of the capacitive coupling circuits includes biasing circuitry configured such that an average control voltage causes a switching device to which it is coupled to be substantially nonconductive.

27. The apparatus of Claim 25, wherein all source switching devices disposed in series between the transfer capacitor and the voltage source, and all output switching devices disposed in series between the transfer capacitor and the output voltage, are capacitively coupled to the charge pump clock output.

28. A method of generating an output supply from a charge pump incorporated within a monolithic integrated circuit by transferring charge from a source voltage to a transfer capacitor ("TC") alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS") circuit is a switching circuit of the charge pump configured to couple the TC to a supply under control of a charge pump clock, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging TCCS circuit under control of a first charge pump clock output; and

b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions such that a voltage of the first charge pump clock output is substantially sine-like.

29. The method of Claim 28, further comprising

c) coupling the TC to the source voltage via a charging TCCS circuit, under control of a second charge pump clock output, during charge periods that nonoverlappingly alternate with the discharge periods; and

d) actively limiting a rate of voltage change of both positive and negative transitions of the second charge pump clock output.

30. The method of Claim 29, wherein the first charge pump clock output is the second charge pump clock output.

31. The method of Claim 30, further comprising controlling all TCCS circuits by means of the first charge pump clock output.

32. The method of Claim 31, further comprising coupling the TC to a connection of the source voltage during a charging period via the charge pump clock output.

33. The method of Claim 28, further comprising limiting a current drive capacity of the charge pump clock output by means of a current limiting circuit.

34. The method of Claim 28, further comprising coupling the first charge pump clock output to a control node of a TCCS circuit via a capacitive coupling circuit.

35. The method of Claim 28, wherein actively controlled TCCS circuits each have an associated control node, the method further comprising coupling the associated control node of each of the actively controlled TCCS circuits to the first charge pump clock output via a corresponding capacitive coupling circuit.

36. The method of Claim 28, wherein a first clock generator driver circuit is a driver circuit functionally incorporated in a first clock generator circuit configured to generate the first charge pump clock output, the method further comprising:

c) limiting source currents from a particular first clock generator driver circuit by means of a first current limiting circuit; and

d) limiting sink currents into the particular first clock generator driver circuit by means of a second current limiting circuit.

37.The method of Claim 36, further comprising limiting the source currents and the sink currents of the particular first clock generator driver circuit to substantially identical magnitudes.

38. The method of Claim 36, wherein the first current limiting circuit comprises a current mirror device, and the second current limiting circuit comprises a different current mirror device.

39. The method of Claim 37, further comprising limiting source currents and sink currents from all first clock generator driver circuits.

40. The method of Claim 28, further comprising generating the first charge pump clock output by means of a current starved ring oscillator including not more than three inverting driver sections coupled in a ring.

41. The method of Claim 28, further comprising coupling the TC to the source voltage or to the output supply in part via a passive TCCS circuit.

42. A method of generating an output supply from a charge pump by transferring charge from a source voltage to a transfer capacitor ("TC") alternately with transferring charge from the TC to the output supply, wherein a TC-coupling switch ("TCCS") circuit is a switching circuit of the charge pump configured to couple the TC to a supply under control of a charge pump clock, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging TCCS circuit under control of a first charge pump clock output;

b) actively limiting a rate of voltage change of the first charge pump clock output during both positive transitions and negative transitions;

c) coupling a first terminal of the TC to a common reference connection of the output supply via a discharge common TCCS;

d) coupling a second opposite terminal of the TC to an output supply connection opposite the common reference connection via a discharge output TCCS; and

e) fabricating the discharge output TCCS to have a control node AC impedance at least double a control node AC impedance of the discharge common TCCS.

43. A method of generating an output supply by alternately transferring charge from a source voltage to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a discharging switch circuit under control of a first charge pump clock output;

b) limiting source current provided to each inverting driver output node of a current starved ring oscillator having not more than three inverting driver stages within a first charge pump clock generator circuit by means of a corresponding source current-limiting circuit; and

c) limiting sink current drawn from each of the inverting driver output nodes by by means of a corresponding sink current-limiting circuit;

wherein the inverting driver output node of one of the not more than three inverting driver stages of the first charge pump clock generator circuit is the first charge pump clock output.

44. The method of Claim 69, further comprising

d) coupling the TC to the source voltage via a charging switch circuit, under control of a second charge pump clock output, during charge periods alternating nonconcurrently with the discharge periods.

45. The method of Claim 69, further comprising coupling a capacitor to the driver output node of the first charge pump clock generating circuit to limit voltage transition rates of the driver output node.

46. The method of Claim 69, further comprising coupling the first charge pump clock output to a control node of the discharging switch circuit and/or to a control node of a charging switch via a corresponding capacitive coupling circuit.

47. The method of Claim 69, further comprising coupling the first charge pump clock output to a control node of the discharging switch circuit and/or to a control node of a charging switch via a corresponding capacitive coupling circuit.

48. The method of Claim 69, further comprising coupling the first charge pump clock output as a signal to a control node of the discharging switch circuit via a network that is not configured to increase rates of voltage change of the signal.

49. A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a TC discharging switch under control of a single phase charge pump clock output that is passively coupled to a control node of the TC discharging switch and substantially isolated from the TC; and

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output that is passively coupled to a control node of the TC charging switch.

50. The method of Claim 49, wherein step a) further comprises coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output.

51. The method of Claim 50, wherein step b) further comprises coupling the TC to the voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output.

52. A method of generating an output supply by alternately transferring charge from a voltage source to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling the TC to the output supply during discharge periods via a plurality of TC discharging switches under control of the single phase charge pump clock output;

b) coupling the TC to the voltage source via a TC charging switch, during charge periods that nonoverlappingly alternate with the discharge periods, under control of the single-phase charge pump clock output;

c) coupling a first TC discharging switch in series between a first node of the TC and a common reference connection of the output supply;

d) coupling a second TC discharging switch in series between a second node of the TC opposite the first node and a connection of the output supply opposite the common reference connection; and

e) fabricating the second TC discharging switch to have a control node AC impedance at least twice as large as a control node AC impedance of the first discharging switch.

53. The method of Claim 49, wherein step b) further comprises coupling the TC to the voltage source via a plurality of TC charging switches under control of the single phase charge pump clock output.

54. The method of Claim 49, further comprising:

c) coupling a second TC to a second voltage source via a second TC charging switch under control of the charge pump clock output; and

d) coupling the second TC to a second output supply via a second TC discharging switch under control of the charge pump clock output.

55. The method of Claim 54, further comprising coupling the charge pump clock output to a control node of each TC charging switch, and to a control node of each TC discharging switch, via corresponding capacitive coupling circuits.

56. The method of Claim 49, further comprising coupling the charge pump clock output to a control node of each actively controllable TC charging switch, and to each actively controllable TC discharging switch, via corresponding capacitive coupling circuits.

57. The method of Claim 49, further comprising incorporating circuitry to reduce voltage change rates during both positive and negative transitions of the charge pump clock output.

58. The method of Claim 49, further comprising:

c) generating the charge pump clock output in a charge pump clock generator circuit having one or more driver circuits, and

d) limiting currents output from each driver circuit of the charge pump clock generator circuit.

59. The method of Claim 58, further comprising:

e) limiting rates of both positive and negative voltage transitions at an output node of one of the driver circuits of the charge pump clock generator circuit by coupling a capacitor to the output node of the driver circuit.

60. A method of generating an output supply within a monolithic integrated circuit by alternately transferring charge for the output supply from a source voltage to a transfer capacitor ("TC"), and from the TC to the output supply, the method comprising:

a) coupling a first charge pump clock output to a control node of a TC charging switch via a first capacitive coupling network that does not conduct a significant portion of the charge for the output;

b) coupling the TC to the source voltage during charge periods via the TC charging switch under control of the first charge pump clock output;

c) coupling a second charge pump clock output to a control node of a TC discharging switch via a second capacitive coupling network that does not conduct a significant portion of the charge for the output; and

d) coupling the TC to the output supply via the TC discharging switch during discharge periods nonconcurrently alternating with the charge periods under control of the second charge pump clock output.

61. The method of Claim 60, wherein the second charge pump clock output is the first charge pump clock output.

62. The method of Claim 61, further comprising biasing each of the capacitive coupling networks such that the TC charging or discharging switch to which it is coupled is nonconductive when the charge pump clock output is at an average value of its time-varying voltage.

63. The method of Claim 62, further comprising coupling the TC to the source voltage during the charge periods via an additional second TC charging switch having a control node capacitively coupled to a corresponding second charge pump output.

64. The method of Claim 63, wherein the TC discharging switch is a first TC discharging switch and is coupled between a first node of the TC and a connection of the output supply opposite a common reference, the method further comprising coupling an opposite second node of the TC to the common reference of the output supply during the discharge periods via a second TC discharging switch having a control node AC impedance no more than half as large as a control node AC impedance of the first TC discharging switch.

65. The method of Claim 62, further comprising coupling the TC to the output supply during the discharge periods via an additional second TC discharging switch having a control node capacitively coupled to a corresponding second charge pump output.

66. The method of Claim 60, further comprising capacitively coupling a control node of each actively controllable TC coupling switch that is incorporated within a charge pump to a corresponding charge pump clock output.

67. The method of Claim 66, wherein all of the corresponding charge pump clock outputs are a common single-phase output.

68. The apparatus of Claim 1, wherein the number of driver sections of the ring oscillator is not less than three.

69. The method of Claim 43, wherein the number of driver sections of the ring oscillator is not less than three.

70. The apparatus of Claim 18, wherein each of the source switching devices and each of the output switching devices is a transfer capacitor ("TC") switching device, each such TC switching device is either an n-channel FET or a p-channel FET, and wherein threshold voltages of all n-channel TC switching devices are substantially similar, and threshold voltages of all p-channel TC switching devices are substantially similar.

71. The method of Claim 49, wherein each TC charging switch and each TC discharging switch is a TC switching device and is either an n-channel FET or a p-channel FET, and wherein threshold voltages of all n-channel TC switching devices are substantially similar, and threshold voltages of all p-channel TC switching devices are substantially similar.

IX. EVIDENCE APPENDIX

The following references relied upon by the Appellants were entered into the record at least when considered by the Examiner on the dates indicated. A copy of each reference is attached.

Each of the following references was cited in an Information Disclosure Statement filed in the U.S. Patent Office on February 10, 2004 and considered by the Examiner on November 17, 2004:

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5. Texas Instruments, "TPS60204, TPS60205, Regulated 3.3-V, 100-mA Low-Ripple Charge Pump, Low Power DC/DC Converters", published February, 2001, Revised September 2001, pages 1 -18.
6. Sam Nork, "New Charge Pumps Offer Low Input and Output Noise" Linear Technology Corporation, Design Notes, Design Note 243, published November 2000, pages 1-2
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Each of the following references were cited in an Office Action by Examiner Terry Englund from the U.S. Patent Office on December 1, 2004:

9. US 5,446,418, issued 08/29/95 to Hara, et al.
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Each of the following references were cited in an Office Action by Examiner Terry Englund from the U.S. Patent Office on August 10, 2005:

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Each of the following references were cited in a Supplemental Information Disclosure Statement filed in the U.S. Patent Office on May 15, 2006, and were considered by the Examiner on May 3, 2007:

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X. RELATED PROCEEDINGS APPENDIX

None.

XI. TABLE OF CASES

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2. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966)
3. *Panduit Corporation V. Dennison Manufacturing Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed Circuit, 1985)
4. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert denied*, 469 U.S. 851 (1984) ("*W.L.Gore*")
5. *Andrew Corp. v. Gabriel Electronics,* 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988)
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